

# **IEUVI Panel Discussion**

September 10<sup>th</sup>, 2017

Organized by  
Paolo Gargini  
Chairman IEUVI

## **Will the advent of 3D monolithic integration eliminate the need for higher lithographic resolution?**

For over 50 years the combination of enhanced lithographic resolution and device structural optimization in conjunction with cell design cleverness have contributed to increase transistor density from one technology generation to the next. Aggressive reduction in the number of defects as a function of time has also increased die yield and allowed cost effective manufacturing of larger dice. Finally, the combination of the above factors with circuit design cleverness has allowed growing the number of transistors at Moore's Law pace.

Practical limits of dynamic power dissipation for microprocessors were reached by the middle of the past decade and the electronics industry was faced with the realization that both the number of transistors and the operational frequency could no longer be simultaneously increased. Faced with this dilemma the electronics industry decided to continue following Moore's Law while limiting any increase in operational frequency to a minimum even though transistors were perfectly capable of operating at much higher frequencies.

2D scaling will reach fundamental physical limits by the middle of the next decade and the semiconductor industry is systematically moving towards new revolutionary solutions to overcome this "red brick wall".

3D monolithic integration of non-volatile memories is already in progress and subsequently 3D monolithic integration of logic and multiple layers of non-volatile memories will allow to continue increasing transistor count at Moore's Law pace and enhance computing performance closer to previous historical rates.

Most of the reports related to the benefits of 3D monolithic integration indicate that many critical features will be controlled by film deposition and etch parameters rather than by lithographic resolution. In fact, several memory companies are already relaxing many of their lithographic requirements.

Faced once again with a critical dilemma should the electronics industry effort concentrate on 3D monolithic integration or towards lithographic resolution enhancements?

Come and find out what the experts recommend, see you there!