Line Width Roughness Control for EUV Patterning

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Resist Technical Work Group meeting 02/12/2012
Controlling line width roughness (LWR) is a critical issue in extreme ultraviolet lithography (EUVL). High sensitivity, high resolution, and low LWR are required for EUV lithography resist. However, it is difficult to realize optimal properties simultaneously through chemical tuning alone. The track process is one of the factors that impacts LWR. Enhancing the track processes used in EUV lithography is necessary to control LWR.

<table>
<thead>
<tr>
<th>Combined Process</th>
<th>Initial Resist Pattern</th>
<th>Post FIRM™ Resist Pattern</th>
<th>Post Smoothing Resist Pattern</th>
<th>Post Etching SiN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CD:29.1nm LWR:4.59nm</td>
<td>CD:29.3nm LWR:4.57nm (0.5%)</td>
<td>CD:29.1nm LWR:4.12nm (10.2%)</td>
<td>CD:34.0nm LWR:3.84nm (16.4%)</td>
</tr>
</tbody>
</table>

2011 SPIE 7969-37
Karen Petrillo, et al.
Outline

- Resist Process LWR Improvement
  - Developer process optimization
  - FIRM™ Process effect
  - Smoothing
  - Combination experiment result
- Through Etch LWR Improvement
- Summary
Developer Process Optimization

- DEV process optimization

- Development process is one of the key factors for LWR improvement.
- LWR was improved by pattern profile control.
- Static-A recipe showed the best result, LWR was improved 7.7%.

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- EUV Resist 75nm
- 32nm Pitch 70nm
FIRM™ (Finishing up by Improved Rinse Material)

FIRM™ Process

Development → Rinse (D.I.W.) → FIRM™ treatment → Dry out → Finish!

TMAH/TBAH

☑ FIRM™ for Pattern Collapse Mitigation

- EUV Resist 75nm
- 28nm HP

![Pattern Collapse](image)

- FIRM™ Extreme10 improve pattern collapse margin by 1.82 Aspect Ratio (Post Development)
- TBAH with FIRM™ Extreme10 combination shows further improvement, pattern collapse margin was drastically improved up to 1.97 Aspect Ratio
FIRM Process effect for LWR

- FIRM for LWR reduction

- LWR was improved up to 7.0% by FIRM process
- The effectiveness depends on FIRM chemical

- CD: 31.9nm
  LWR 5.22nm
- CD: 31.3nm
  LWR 5.03nm
- CD: 31.9nm
  LWR 4.85nm

- 3.5% improved
- 7.0% improved

- EUV Resist 75nm
- 32nm Pitch 70nm
Smoothing Process

- Resist patterning
- Smoothing
- Bake

Smoothing Baseline Result

- Pre Smoothing:
  - CD: 32.8nm
  - LWR: 5.02nm
  - Post CDU: 1.73nm

- Post Smoothing:
  - CD: 33.4nm
  - LWR: 4.49nm
  - 10.6% improved
  - Post CDU: 1.35nm

- Smoothing process improved LWR 10.6% with no huge impact to average CD or CD uniformity
- There is no significant differences on x-section images
Combination Experiments

Coater/Developer
- System: CLEAN TRACK ACT™ 12 (Tokyo Electron LTD)
- CLEAN TRACK™ LITHIUS Pro™ V (Tokyo Electron LTD)
- Resist: EUV resist material, Film thickness 75nm on Si
- Target CD: 32nm Pitch 70nm
- Developer solution: TBAH
- Rinse solution: FIRM™ Extreme10

EUV Exposure tool
- System: alpha demo tool (ASML)
- Illumination: N.A.=0.25 σ=0.5 Conventional

Measurement
- SEM: Hitachi CG4000

Measurement settings
- ITRS Recommendation
  1. Inspection area L≥2um
  2. Measurement ΔL≤10nm

- Rectangular magnification
- Sampling number was optimized by using 95% interval confidence analysis

- Smoothing: Conventional Smoothing Scheme
- Smoothing Scheme2: Fine Tuning Smoothing Scheme
<table>
<thead>
<tr>
<th>Process</th>
<th>Initial</th>
<th>Developer Optimization</th>
<th>FIRM™</th>
<th>Smoothing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process-A</td>
<td>LWR:5.20</td>
<td></td>
<td>10.4%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CD:32.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process-B</td>
<td>LWR:4.78</td>
<td></td>
<td>11.9%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CD:32.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process-C</td>
<td>LWR:4.71</td>
<td></td>
<td>11.5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CD:32.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process-D</td>
<td>LWR:4.68</td>
<td></td>
<td>16.7%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CD:32.0</td>
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</table>

- Individual techniques are additive techniques and those are available for combination process
- Smoothing process improves LWR 10.4-11.9%, and Smoothing scheme2 improves LWR 16.7%
- Process-D shows the best result, LWR was improved **25.0%**, final LWR was **3.90nm**

- EUV Resist 75nm
- 32nm Pitch 70nm
Result Plots

* Number: LWR Improved% from A.Initial

- DEV optimization, FIRM™ and Smoothing results show statistically significant differences
- All combined Process-D shows the best result; LWR was improved 25.0%, final LWR was 3.90nm
Through Etch Experiments

Through Etch Experiments Process Flow

- Initial LWR
- Reference
- Process-D
- DEV Optimization
- FIRM™
- Smoothing Scheme2
- Etch Smoothing
- Post LWR

Coater/Developer
- System: CLEAN TRACK ACT™ 12 (Tokyo Electron LTD)
- CLEAN TRACK™ LITHIUS Pro™ V (Tokyo Electron LTD)
- Resist: EUV resist material, Film thickness 75nm on Si
- Target CD: 32nm Pitch 70nm
- Developer solution: TBAH
- Rinse solution: FIRM™ Extreme10
- EUV Exposure tool
- System: alpha demo tool (ASML)
- Illumination: N.A.=0.25  σ=0.5 Conventional
- Measurement
- SEM: Hitachi CG4000
- Etching system
- System: Tactras™ (Tokyo Electron LTD)

Experiments stack layer

- EUV Resist (75nm)
- SiARC
- OPL
- SiN
- SiON
- Si

Etch stop on Si

Resist Technical Work Group meeting 02/12/2012
Shinichiro Kawakami/TTCA/CT
Through Etch LWR improvement

- EUV Resist 75nm
- 32nm Pitch 70nm

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<thead>
<tr>
<th></th>
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<th>Developer Optimization and FIRM™</th>
<th>Resist Smoothing</th>
<th>Post Etch Smoothing</th>
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<tbody>
<tr>
<td>Baseline</td>
<td>CD:35.2</td>
<td>LWR:4.66</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process-D with Etch Smoothing</td>
<td>CD:33.3</td>
<td>LWR:4.26 8.6%</td>
<td>CD:33.4</td>
<td>LWR:3.59 23.0%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.0%</td>
<td>15.7%</td>
<td>7.2%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.6%</td>
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- Single Etch smoothing improved LWR 12.0%
- Resist process LWR improvement was confirmed through etch LWR, improvement was increased **16.5%** from single Etch Smoothing
- Process-D with Etch Smoothing showed **28.5%**, final LWR achieved **3.33nm**

* * Number: LWR Improved% from A.Initial
Profile of post smoothing is greatly improved over baseline profile, pattern surface is smoother.
Profile of post etch, Process-D shows slightly better LWR profile in visually.
Power Spectral Density Analysis

- DEV process optimization and FIRM™ are relatively effective in middle frequency regions improvement.
- Smoothing process shows improvement in wider region of frequency, especially from middle to high.
- Etch Smoothing shows improvement in middle frequency region.
Summary

- Three techniques were found for LWR improvement; DEV process, FIRM™ and Smoothing
  - LWR is improved up to 7.7% by development process optimization
  - FIRM™ process up to 7.0% LWR improvement
  - Smoothing process improved LWR 10.4-11.9%. Smoothing scheme 2 shows further improvement, the improvement is 15.7-16.7%
- The combination process shows 25.0% LWR improvement on resist process
  Additive effect was confirmed in all techniques combination experiments
- Resist process LWR improvement was transferred in post Etch LWR, improvement increased 16.5% from Etch Smoothing only
- All combination process shows 28.5%, final optimized LWR achieved was 3.33nm

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<th>Initial (Resist Pattern)</th>
<th>Developer Process Optimization with FIRM™ (Resist Pattern)</th>
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<tr>
<td>CD:35.2</td>
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Combined Process

- CD:35.2
- LWR:4.66
- 8.6%

- CD:33.3
- LWR:4.26 8.6%
- 15.7%

- CD:33.4
- LWR:3.59 23.0%
- 7.2%

- CD:40.1
- LWR:3.33 28.5%
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Thank you for your attention