EUV Resist Pattern Collapse Status

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Outline

Assessment of resist collapse at Berkeley MET
- Resist collapse status of SMT1/2/3/4 EUV resists
- Pattern fidelity of EUV SMT1/2 resist
- Pattern fidelity of SMT1 and SMT2 resist through focus
- Pattern fidelity of EUV SMT3 resist

Assessment of resist collapse at ADT with SMT3 resist
- Process window at 32nm HP patterning without underlayer
- Process window at 32nm HP patterning with underlayer
- Photo process window at 28nm HP with underlayer

Summary
Pattern Fidelity of EUV SMT1 Resist

- Coating Resist Thickness: 50nm
- Substrate: HMDS on bare Si
Pattern Fidelity of EUV SMT2 Resist

- SMT02
  - 26nm HP
  - 24nm HP
  - 22nm HP
  - 20nm HP

- Mag. 200K
  - Aspect ratio: 1.92

- Mag. 400K
  - Aspect ratio: 2.08
  - Aspect ratio: 2.27
  - Aspect ratio: 2.5

- Coating Resist Thickness: 50nm
- Substrate: HMDS on bare Si
Pattern Fidelity of EUV SMT3 Resist

- Coating Resist Thickness: **43nm**
- Substrate: SMTUL1 underlayer on bare Si
Resist Collapse Status of SMT1/2/3/4 EUV Resists

<table>
<thead>
<tr>
<th>Aspect ratio</th>
<th>28nm HP</th>
<th>26nm HP</th>
<th>24nm HP</th>
<th>22nm HP</th>
<th>20nm HP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMT01</td>
<td>1.78</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMT02</td>
<td></td>
<td>1.92</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMT03</td>
<td></td>
<td></td>
<td>2.08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMT04</td>
<td></td>
<td></td>
<td></td>
<td>2.27</td>
<td>2.5</td>
</tr>
</tbody>
</table>

- Resist Thickness: 50nm

We need to improve resist collapse to ensure fullfield patterning feasibility
Resist Collapse Status of EUV Resists

Resist Thickness: 50nm

No Collapse HP (nm)

Resist Samples

A B C D E F G

Aspect Ratio

0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0

Resist Samples
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Assessment of resist collapse at ADT with SMT3 resist
- Process window at 32nm HP patterning without underlayer
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Summary
Process Window at 32nm HP Patterning **without Underlayer**

- DOF: 160nm @ Best Focus
- EL: 13% @ Best Dose
Resist Collapse Improvement with Underlayer

- SMT3 resist, 60nm thickness on hardmask wafer
- 32nm HP patterning; ADI CD 29nm
Process Window at 32nm HP Patterning with Underlayer

- **DOF**: 200nm @ Best Focus
- **EL**: 18.5% @ Best Dose
Photo Process Window at 28nm HP with Underlayer

- DOF: 120nm @ Best Focus
- EL: 13% @ Best Dose
Summary

- Aspect ratio of best EUV resist was 1.92 at MET

- Aspect ratio of current EUV resist was less than 1.8 considering process window at ADT without underlayer

- Aspect ratio of current EUV resist was 2.0 considering process window at ADT using underlayer

- Resist collapse is major issue to resolution enhancement when considering effective process window at ADT

- Resist collapse need to be improved for EUV manufacturing and EUV extendibility
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Thank you for your attention