

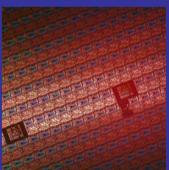
Accelerating the next technology revolution

IEUVI Resist TWG October 2, 2008 Focus Topic Intro: Optimizing RLS?



Jacque Georger - EUV Resist Project Manager







EUV Resist RLS Targets

EUV Resist Specifications	32nm hp	22nm hp
Resolution (lines 1:1, nm)		
½ Pitch	32	22
MPU Gate	21	15
LWR (nm, 3σ)		
8% of MPU Gate	1.7	1.2
10% of DRAM HP	3.2	2.2
Photospeed, EUV(mJ/cm²)	10	10

Focus Topic Intro: Keys to Optimizing RLS in EUV?



- Control/Minimize Diffusion (<hp <L, >Es)
 - Quencher & Acid: Q&A Diff. Lengths & Ratio, Q/A Loading
 - Dynamic Diff. Lengths: Q&A Diff. > in Expose area Vs Un-Exposed
 - Processing bakes: < PEB Temp & Time, > PAB Temp
- Smaller or Dynamic Inhibiting Platforms (<hp, ≤L, ~Es)
 - Inhibitors: <Mw, Tighter Mw distribution & Molecular distribution
 - Dynamic size Inhibitors: Large → Small, or Small → Large
- Increase Film Quantum Yield (~hp, ~L, <Es)
 - PAG loading, Better Utilize available Secondary e-
- Develop (<u><</u>hp, <L, <u>< ></u>Es)
 - Developer: Conc., Surface Energy, Organic, Additives
- Post Develop & Pattern Transfer (~hp, ≤L, ~Es)
 - Resist Sliming/Smoothing: Dry Etch, Rinse?
 - Optimize Hard Mask & Substrate Transfer Etch for LER/LWR?
- Aerial Image Improvement (<hp, <L, <Es)
 - Higher NA & Brighter Source