EUV resist roadmap discussion

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Resist TWG meeting 3/01/2007

Outline

- Resist roadmap discussion
  - Timing
  - Figure of Merits

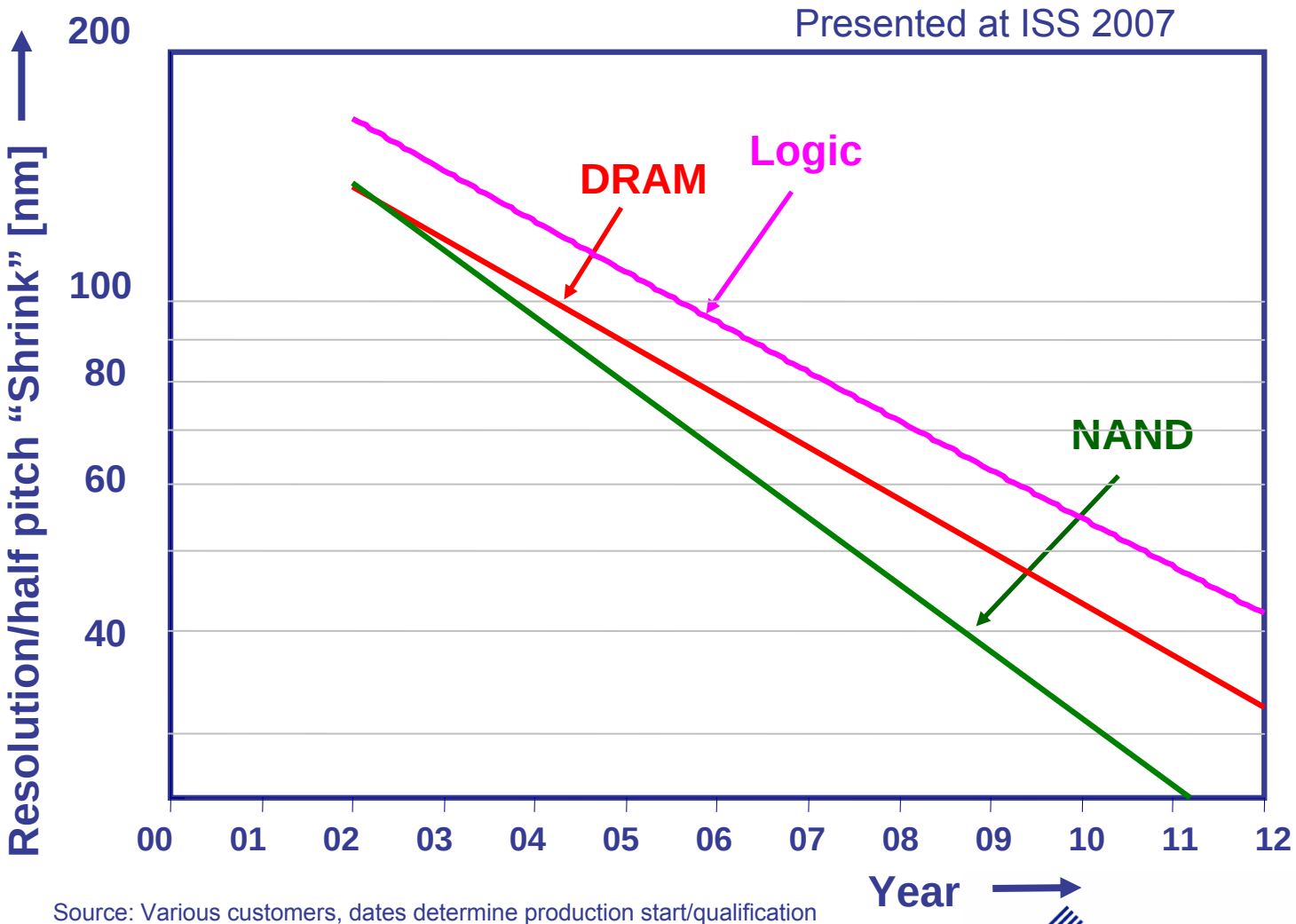
EUV Resist Specification Roadmap

Specifications	Alpha (2006-07)		Beta (2009-10)		Production (2012-13)	
	Spec	Current**	Spec	Comment	Spec	Comment
Resolution 1:1	45nm	35nm/45nm (C/S)	32nm		32nm	
Resolution contacts	55nm	TBD	40nm		35nm	
Resolution Isolated Lines	32nm	30nm/40nm (C/S)	25nm		21nm	
Depth of Focus	200nm	100nm for 35-nm 1:1 200nm for 50-nm 1:1	225nm	Dense and isolated; DOF at 10% exposure latitude	225nm	Dense and isolated; DOF at 10% exposure latitude
Photospeed (mJ/cm^2)	10 mJ/cm^2	21mJ/cm^2 E-size @ 50-nm 1:1	10mJ/cm^2	Assuming ~30 wph	10mJ/cm^2	Assuming > 100 wph if 5 mJ/cm^2, 115W intermediate focus
Line Width Roughness (3 σ)	< 4 nm (LER)	~4 nm @ 50-nm 1:1 ~7 nm @ 35-nm 1:1	< 2.5nm		< 1.7 nm	LWR < 8% etched gate length; gate length = 18 nm
Wall Profile Angle	>85°	80° @ 50-nm 1:1	> 85°	Measure cross-sections	> 85°	Measure cross-sections
Outgassing	4.7E13 molecules/cm2-sec	1.60E+13	TBD		TBD	
Pattern Collapse	>3	None observed	>3	Aspect ratio 3:1 for all structures	>3	Aspect ratio 3:1 for all structures
Unexposed Film Thickness Loss	< 10%	10nm	< 5%		< 5%	
PEB Sensitivity	< 2.5 nm/deg C	TBD	<1.5 nm/deg C		< 1 nm/deg C	
Delay Stability @ < 1ppb amine	30min	TBD	30 min	a) pre-exposure, b) under vacuum, c) post-exposure	30 min	a) pre-exposure, b) under vacuum, c) post-exposure
Etch Resistance	Similar to novolak	TBD	Similar to novolak		Similar to novolak	

**Measured top down values for Rohm and Haas resist MET-1K.
C/S=cross section **Green** = spec is met, **Orange** = spec is not met

ASML

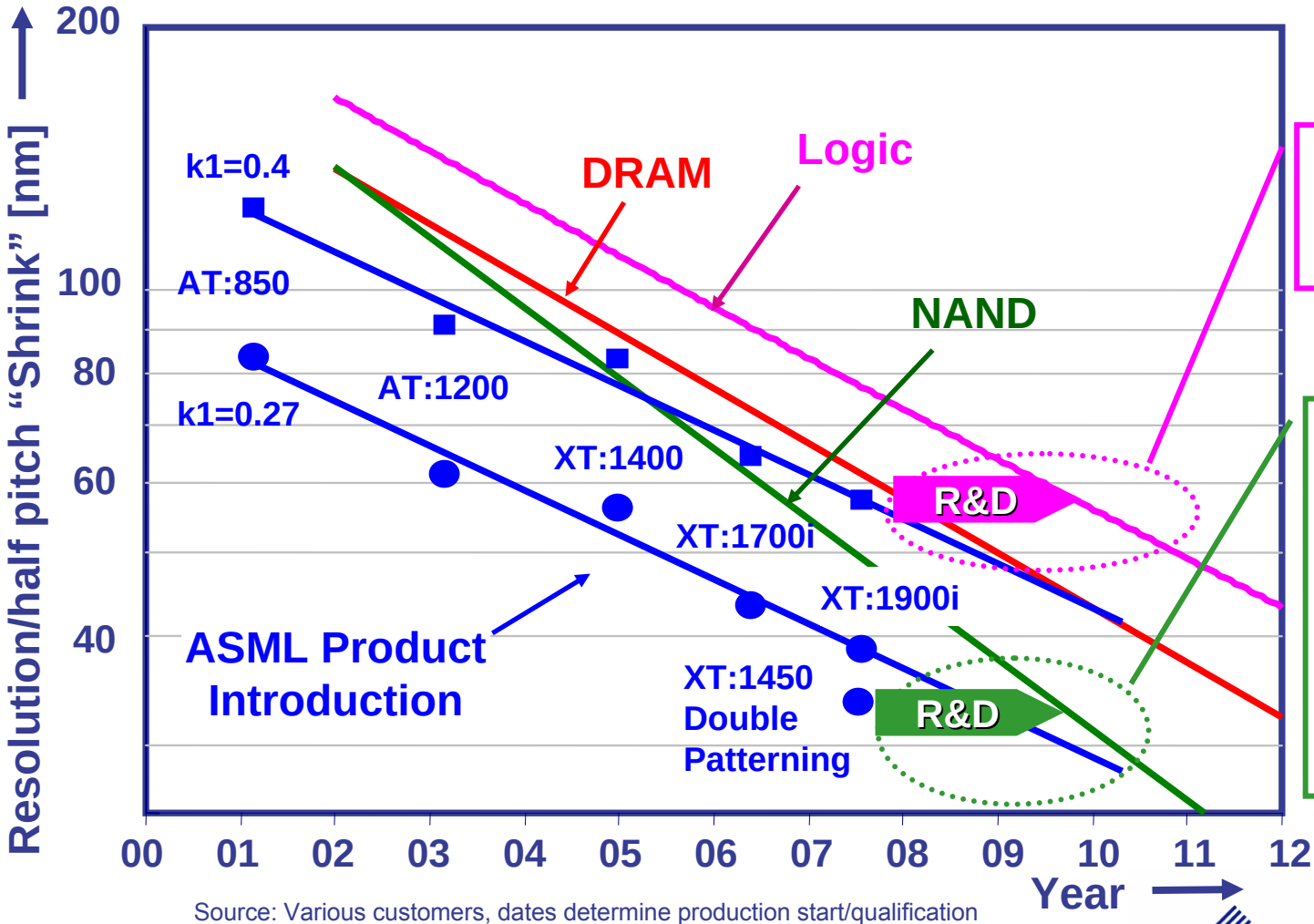
Shrink rates for Logic, DRAM, and NAND flash



Source: Various customers, dates determine production start/qualification

ASML

Shrink rates for Logic, DRAM, and NAND flash versus tool introduction at k_1 0.27 and 0.40



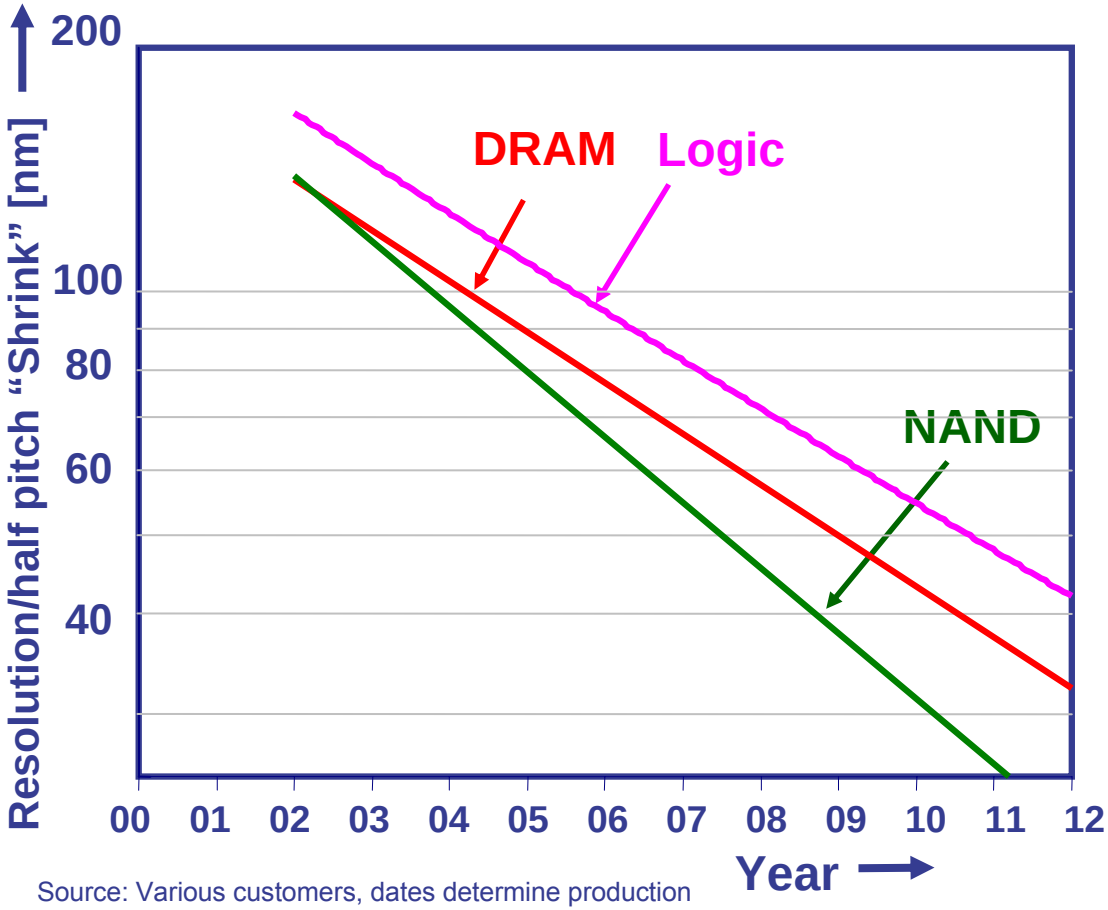
Litho technology will allow Logic to shrink

To enable continued shrink for memory: EUV is needed, Double Patterning to bridge gap until EUV mature

Source: Various customers, dates determine production start/qualification

ASML

Shrink rates for Logic, DRAM, and NAND flash



Source: Various customers, dates determine production start/qualification

year	Half pitch
2005	65
2007	45
2009	32
2011	22
2013	16
2015	11

Infrastructural requirements

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Imaging Figure of Merits

- Currently specified:
  - Resolution, DoF@10%, Sensitivity, LWR
  - Arbitrary, Tool/ illumination dependent
- Ideas
  - Resist induced contrast loss
  - Others?
- Discussion
  - Measure MTF if aerial contrast of tool is known
  - Should move 32 nm earlier? 2010?