EUV PELLICLE TWG, MAASTRICHT, THE NETHERLANDS
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EUV PELLICLE MANUFACTURABILITY

Ted Liang

IMO
Intel Corporation

Main Messages:

- Progress is being made in EUV pellicle development (as in ASML presentation)
- Intel wants to use EUVL for production as soon as possible (as it is ready to support technology development)
- Concerns exist about the extendibility of the current solution with respect to high volume manufacturing (HVM) and throughput
- For HVM, we need a robust and commercial pellicle platform that improves transmission, lifetime, and other key performance parameters

Remarks for EUV Pellicle in HVM

- **Mask shops and suppliers have developed BKMs (best known methods) in ArF pellicle materials, tooling and operations over many years of experiences of what worked well and what to avoid, notably**
  - Integrated pellicle from suppliers (film + frame + filters)
  - Simple handling and mounting (attachment) at mask shop (keep the process clean)
  - Post-pellicle inspection (pattern surface and pellicle surface) to directly monitor what happens beneath the pellicle

- **It is desirable to adapt as many as possible these BKMs in EUV pellicle development and commercialization**
  - This will help to reduce technical and schedule risks for pellicle implementation in HVM
  - Opportunities exist to introduce technologies to mitigate these risks/concerns

Pellicle Film Performances

- **Lifetime: commensurate with source power and WPH throughput of NXE in production**
  - Transmission >90%
  - Thermal load: equivalent to 250W
  - Tens of thousands of wafers
- **Uniformity: T <0.2%**
- **Defects in and on the film**
  - Particle inspection tools exist today to support process development
  - Development of mechanically robust pellicle films might allow particle blow-off
  - Methods for removal of fall-on particles on thin film membranes desired

Pellicle Mounting

- **The entire process must be clean (no adders)**
  - Any mounting flow needs to avoid adders during the mounting process
  - Frame venting solution needs to maintain adder-free environment beneath the pellicle

- **Mounted pellicle needs to have no impact to mask flatness from pellicle induced stress**

- **Any new mounting technology needs to be consistent with current NXE platform design**

Post-pellicle Mask Qualification

- **Direct qualification with through-pellicle inspection (TPI) in mask shop**
  - The industry standard, the only known effective way to guarantee integrity of a pattern under pellicle (particle adders, contamination, PID)
  - Optical inspection not capable (low transmission to long wavelengths >400nm)
  - TPI only possible with actinic EUV light (13.5nm), however, actinic pattern mask inspection (APMI) will not be ready in time to intercept EUV insertion due to long development time
- **For long term, TPI is needed to directly monitor what happens to mask patterns without removing the pellicle**
  - Detect contamination on mask surface before impacting wafer yield
  - Increase productivity by avoiding the cycle of wafer print
- **APMI development needs to start now and occur in parallel with EUV introduction**
- **Indirect qualification with high resolution wafer inspection in the Fab**
  - Enable EUV insertion before TPI becomes available
  - Exchangeable pellicle design allows mask re-clean and inspection

Ref: Mark Phillips/Intel, 2015 PMJ

Same slide shown in 2015 BACUS

Re-pelliclization

- **It is desirable to preserve and re-use pellicles as much as possible from re-pell cycles**
- **Pellicle materials, tooling and demounting procedure need to enable re-pell process**
- **The re-pell may be triggered by the following events**
  - Particles added on the mask during mounting
  - Particles on pellicle that may not be removed
  - Contamination developed on the mask
  - Pellicle degraded or damaged

- **Mask clean with glue-removal process will be needed at each re-pell cycle**

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Thank you for your attention!