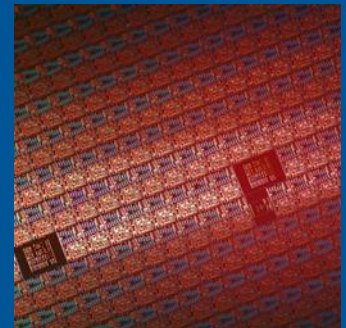


Accelerating the next technology revolution

# Driving the Industry to a Consensus on High-NA EUV

Patrick Kearney

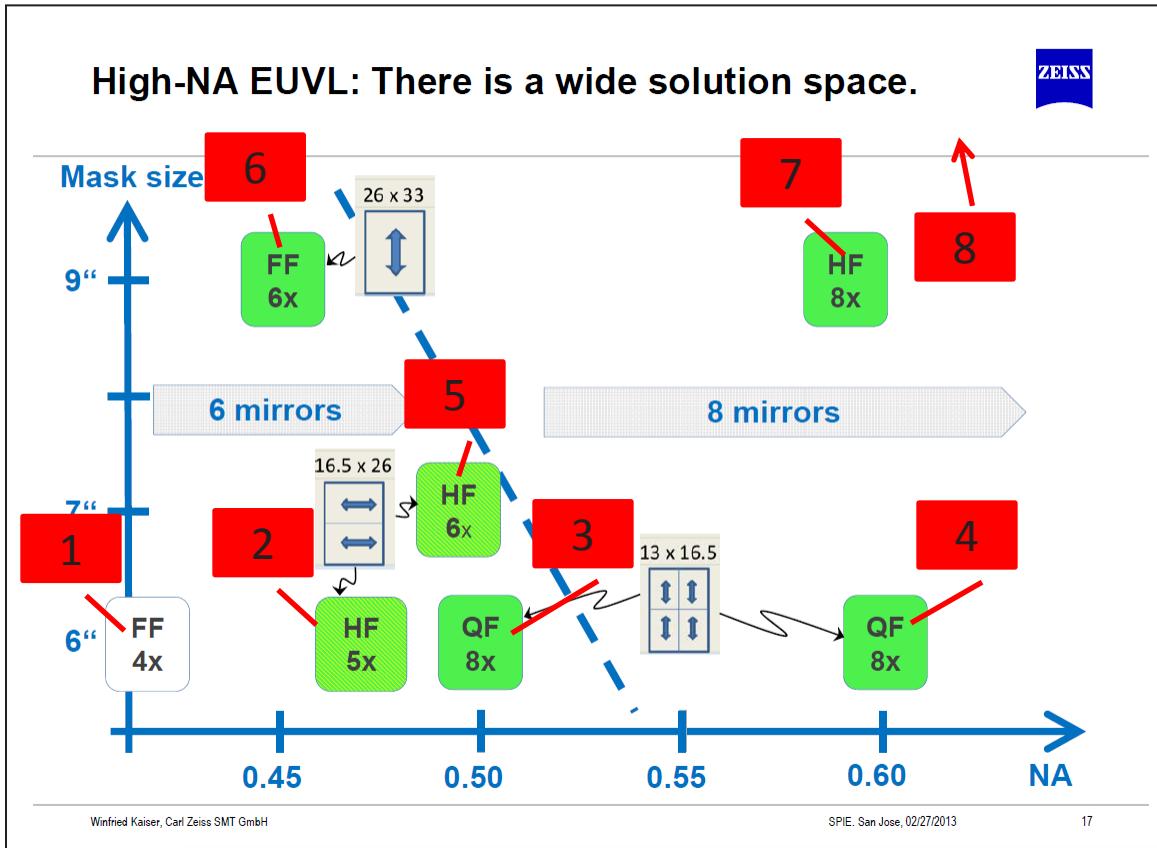


# The High-NA EUV Team



- *Obert Wood, Globalfoundries*
- *Eric Hendrickx, IMEC*
- *Greg McIntyre, IBM*
- *Jan van Schoot, ASML*
- *Winfried Kaiser, Carl Zeiss*
- *Soichi Inoue, EIDEC*
- *Frank Goodwin, SEMATECH*
- *Stefan Wurm, SEMATECH*

# Potential solutions



Throughput/mirrors:  
8 mirror systems should have ~40% of the throughput of 6 mirror systems.

Throughput/field size:  
Assumed HF reduced throughput to 74% and QF reduced throughput to 55%.  
Throughput is just these two factors multiplied, represents throughput relative to case 1.

Case	Magnification	Field size	Mask size	"Resolution"	NA	Coatings	N mirrors	Throughput
Case 1	4x	FF	6 inch	9.9 nm	0.41	Advanced	6	100%
Case 2	5x	HF	6 inch	8.6 nm	0.47	TBD	6	74%
Case 3	8x	QF	6 inch	8.1 nm	0.50	Standard	6	55%
Case 4	8x	QF	6 inch	6.8 nm	0.60	Standard	8	22%
Case 5	6x	HF	7 inch	8.1 nm	0.50	Standard	6	74%
Case 6	6x	FF	9 inch	9.0 nm	0.45	Standard	6	100%
Case 7	8x	HF	9 inch	6.8 nm	0.60	Standard	8	30%
Case 8	8x	FF	12 inch	6.8 nm	0.60	Standard	8	40%

# Tradeoffs



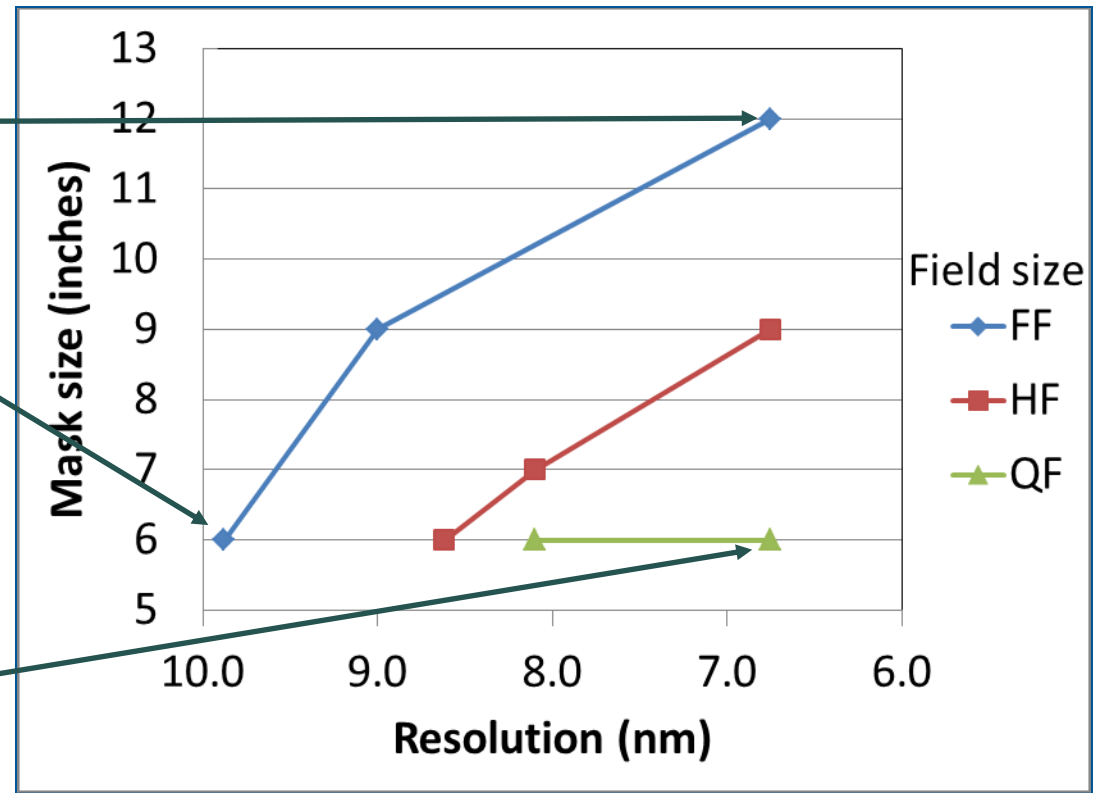
- Resolution
- 6" mask
- Full wafer field

Industry must give up one

Give up 6" mask

Give up resolution

Give up Full wafer field



# SEMATECH High-NA EUV Survey

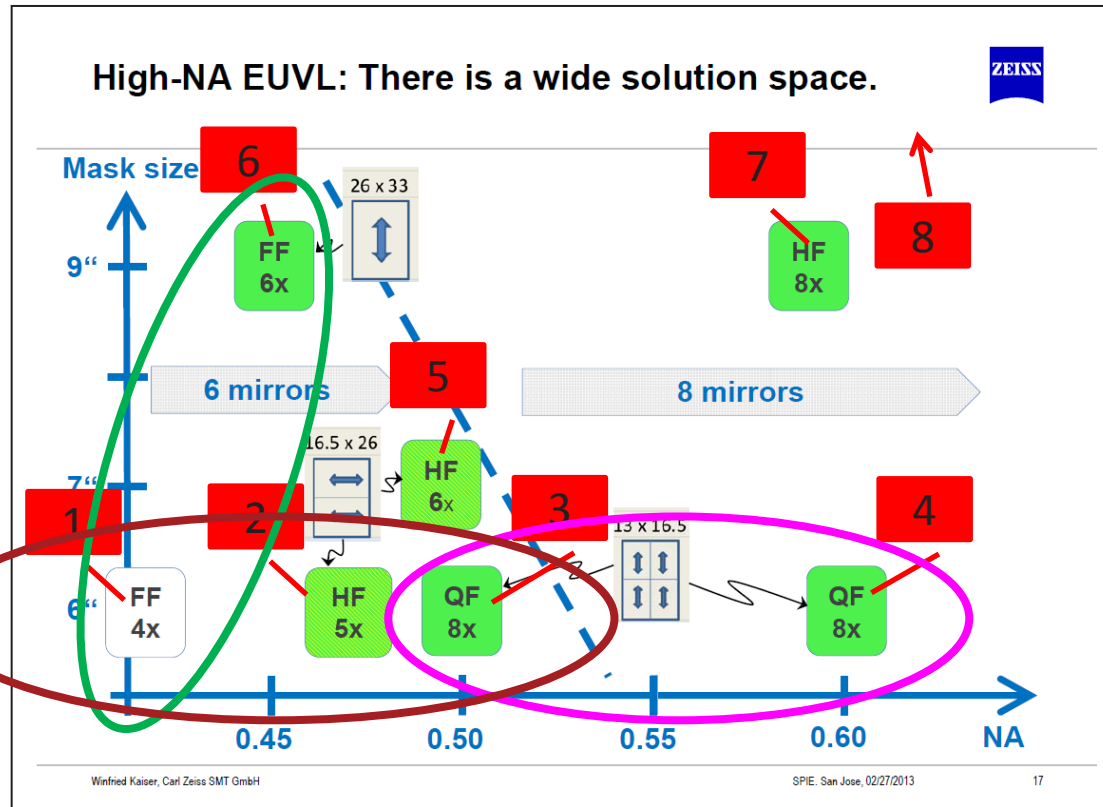
*Get Industry Perspective on High-NA EUV*



- Four anonymous surveys were conducted with each of the following stakeholder groups
  - Chip makers: 8 of 9 companies responded
  - Mask makers: 9 of 11 companies responded
  - Stepper suppliers: 4 of 4 companies responded
  - Mask tool/material suppliers: 18 of 22 companies responded
- All four surveys had excellent industry participation
- Survey conducted in Q2-2013

# All Companies Feedback

## High-NA Preferences



FF = Full Field  
 HF = Half Field  
 QF = Quarter Field

- Some overlap between chip makers and mask makers
- Some overlap between mask makers and equipment and material makers
- But there is no common ground yet between all three groups

# High-NA EUV Survey Conclusions



- Chip makers want full field solutions
  - Beyond 10 nm half-pitch this will require higher magnification and a larger mask
- Chip makers are evenly split between 9-inch and 12-inch mask preferences
  - 9-inch masks will support Case 6 for 9 nm resolution.
  - 12-inch masks will support Case 8 for 7 nm resolution
  - The industry only wants one mask size change
- Mask makers and equipment/material makers prefer to stay with the current 6-inch mask size
  - A switch to 9- or 12-inch mask sizes is expected to take 3 to 6 years
- Mask equipment/material makers do not expect fundamental changes required to their technology to accommodate larger mask sizes

# July 9<sup>th</sup> Meeting Summary



- Mask equipment suppliers will not invest in a new mask size without more consensus from the chipmakers
- Chipmakers seem to be waiting for EUV to be successful before placing bets on High-NA EUV
- Since a size transition is expected to take 3-6 years, this either:
  - Forces a delay of High-NA EUV  
or
  - Limits initial High-NA EUV to the 6” mask size solutions.



# Summary



- SEMATECH has laid out the options for High-NA EUV
- SEMATECH has surveyed the industry and found there is disagreement between the chipmakers, mask makers and supply chain about how to proceed
  - Equipment suppliers and mask makers prefer solutions that retain 6" masks
  - Chipmakers want full field solutions and at high resolution that implies larger masks
- If chipmakers don't push for a larger mask soon, we may end up with a delayed implementation of High-NA EUV or limit ourselves to 6" masks
- There is a side meeting here at the EUV Symposium to get the key stakeholders in the same room to discuss how to move forward

# Why consider High-NA EUV now?



- Scanner roadmap predicts end of 0.33 NA single patterning at 13 nm feature size
  - For smaller features EUV double patterning or high-NA EUV is required
- A transition to high-NA EUV requires ~5 years to prepare
  - If high-NA EUV should be needed in 2018/19 then a decision on the high-NA EUV path has to be made by YE 2013
- Transitioning to high-NA EUV is an industry decision and needs to be broadly supported. This requires:
  - Understanding of what is and what is not acceptable to EUV stakeholders (chip makers, mask makers, tool and materials suppliers)
  - Stakeholders need to develop their own internal assessment and position with respect to high-NA EUV
  - Company positions on high-NA EUV need to be shared so that, as an industry, we understand where we agree and where we differ

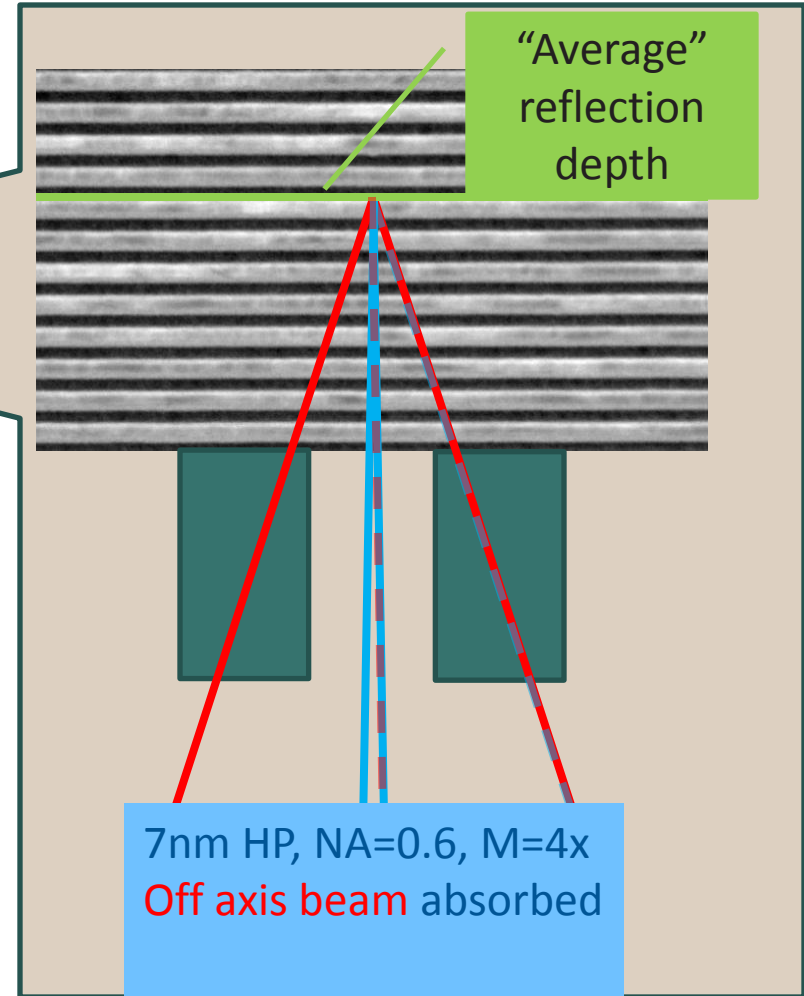
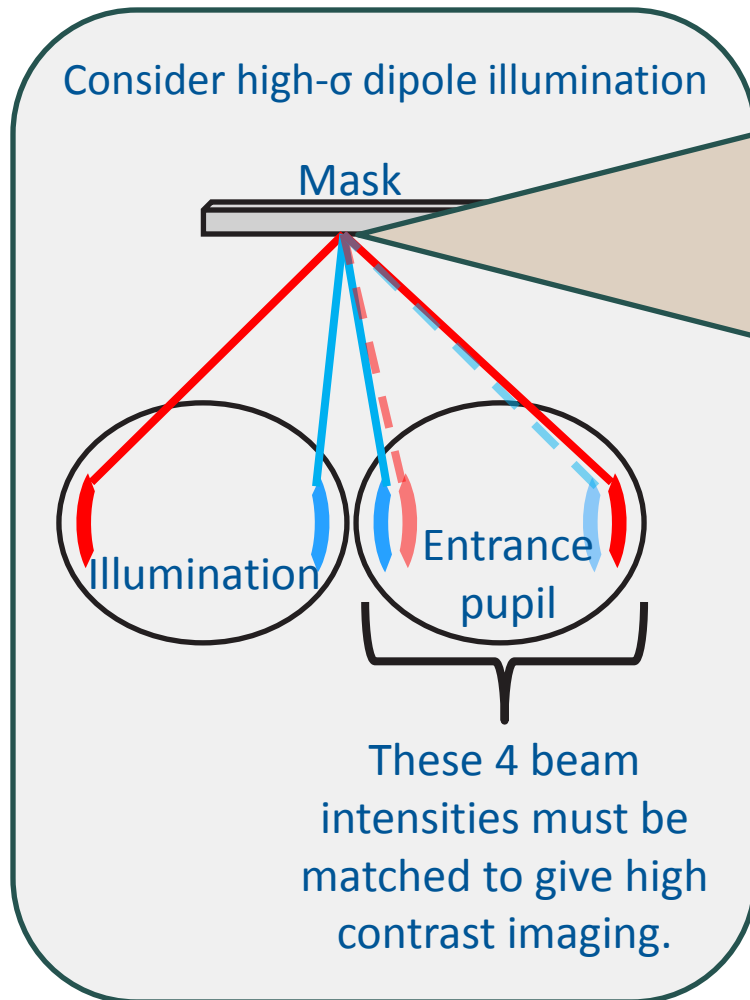
# Team driving industry to a decision

## *Timeline / Milestones*



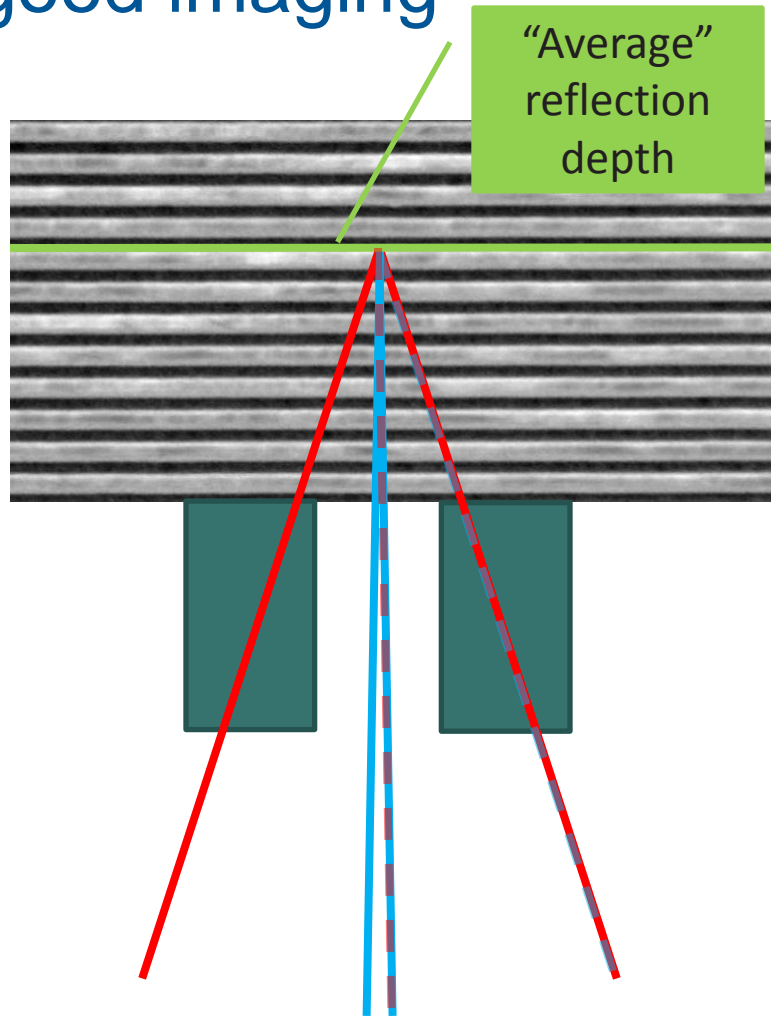
- Q1 2013: Assess current status of high-NA EUV discussion
  - Review literature, assess the possibilities
  - Develop shared understanding of the current high-NA EUV options as they are being discussed
- Q2 2013: Share state of current high-NA EUV industry discussion with stakeholders / get early feedback
  - Face-to-face meetings with all stakeholders
  - Survey all stakeholders for their views
- July 9<sup>th</sup>: SEMATECH High-NA EUV Workshop at SEMICON West.
  - Share industry survey results on high-NA EUV
  - Stakeholders share their perspective and learn about the perspective of others
- Q3-Q4 2013: Industry discussion
  - Narrow options, drive industry consensus, and identify differences
  - Follow-up industry workshop co-located with EUVL Symposium
- End of 2013:
  - Achieve industry consensus on what high-NA EUV will look like  
or
  - Determine where the differences are

# Image quality requires increasing demagnification as NA is increased

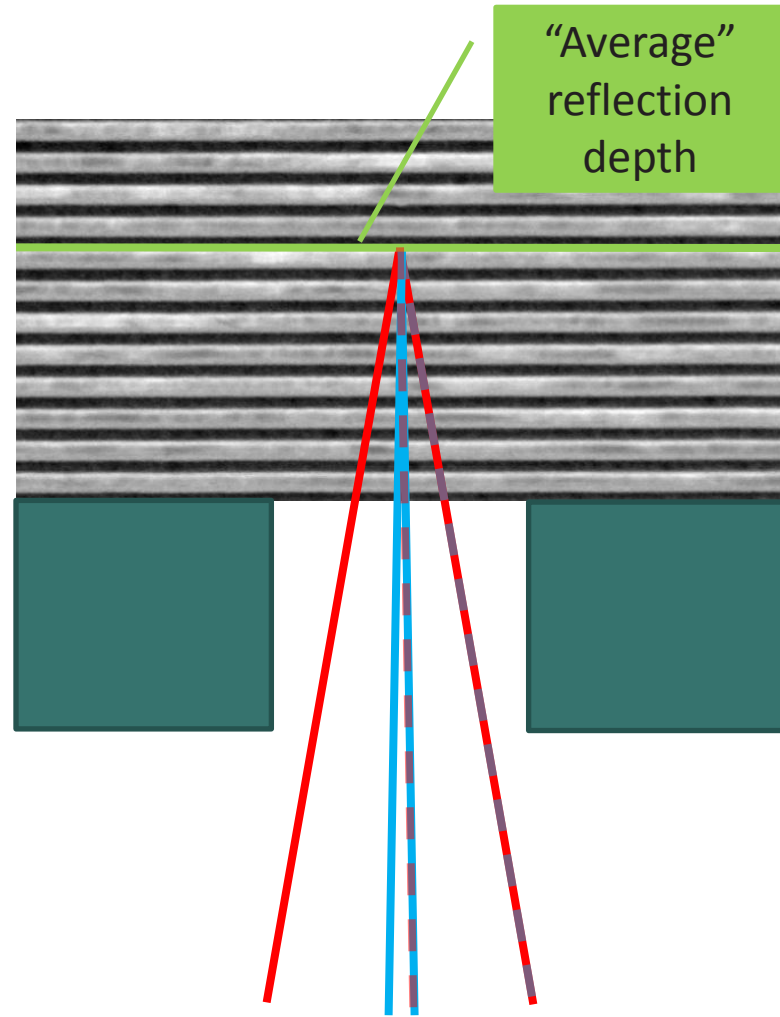


Off axis beam is absorbed, poor image quality.

# Increasing demagnification can bring back good imaging



7 nm HP, NA=0.6, M=4x  
Off axis beam absorbed



7 nm HP, NA=0.6, M=8x  
Off axis beam reflected

# Field size and magnification



- Since the magnification increases, either the mask gets bigger or the wafer field gets smaller.
- Consider 3 cases for wafer field:
  - Full Field (FF) – 26x33 mm
  - Half Field (HF) – 16.5x26 mm
  - Quarter Field (QF) – 13x16.5 mm
- Consider 3 cases for mask size:
  - 6” square
  - 9” square
  - 12” square

Mask size for combinations of field size and magnification

Field size	4X	6X	8X
FF	6”	9”	12”
HF	6”	9”	9”
QF	6”	6”	6”

# Limiting Factors—Optical design



- High-NA large field steppers require more mirrors (8).
  - 8 mirror steppers will have ~40% of the transmission of 6 mirror steppers
  - 8 mirrors are required for  $NA = 0.6$  steppers

# Design parameters



- Feature size &  $k_1$  → minimum NA
  - Imaging requirements & NA → minimum demagnification
  - Demagnification & field size → minimum mask size
  - NA, demagnification & field size → number of mirrors
  - Number of mirrors & field size → stepper throughput
- 
- The “free” parameters are field size, demagnification at each NA
  - Useful demagnifications range from 4x to 8x



# Cost drivers



- Stepper
  - Stepper throughput will drive cost in operation
    - Larger wafer fields increase throughput
    - Fewer mirrors increases throughput
  - Higher demagnification, higher NA, larger field steppers will be more expensive, but this is anticipated to have a relatively small effect
- Mask size
  - Changing mask size will be expensive, requiring retooling throughout the supply chain

# Summary of High-NA Options



- Increasing NA much above current levels will require increased stepper demagnification
- Keeping 6" masks will require reducing the wafer field size
- Alternately, there are larger field solutions possible for 9" and larger masks
- We have presented an overview of the possible solutions
- Our task is to drive the industry toward consensus by YE 2013