EXPERIENCES WITH THE **"CLEAN RETICLE HANDLING"** PATH TOWARDS HVM NEEDS

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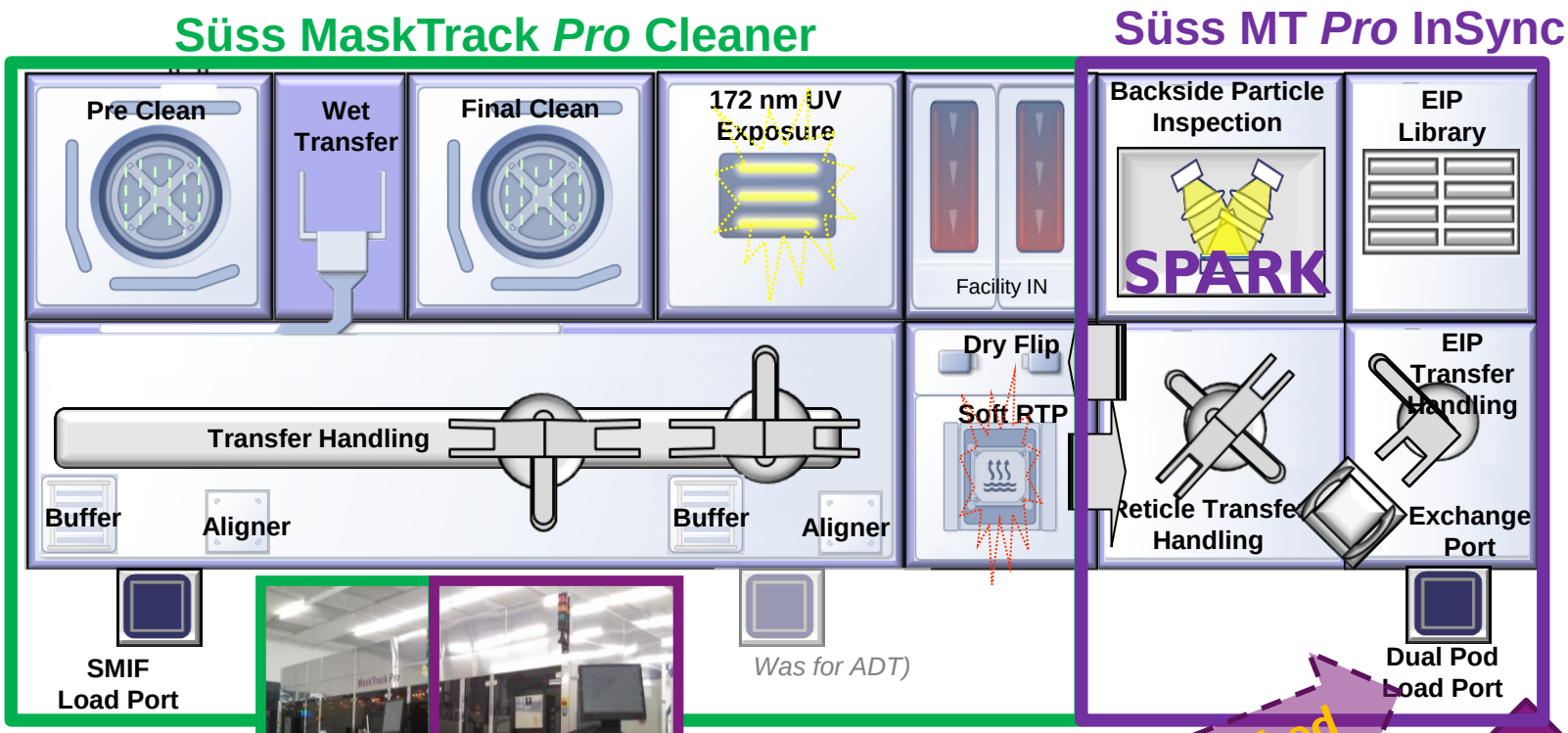
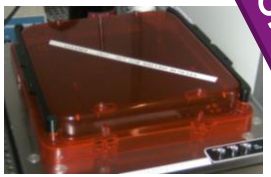
REMINDER: AVAILABLE INFRASTRUCTURE INTEGRATING CLEANING, BACK-SIDE INSPECTION AND AUTOMATED HANDLING OF NXE3100 RETICLES





RSP200

Shippable EUV POD to be established

EUV POD Type A

Mask shop

NXE3100

BASELINE WAY-OF-WORKING

New NXE3100 reticles

- The reticle is received from the mask shop in ...
  - ... shipping box: manual load into RSP200, auto transfer into EUV pod on InSync
  - ... RSP200: auto transfer into EUV pod on InSync
  - **... EUV pod: only exceptionally used for shipping so far → EVALUATE !!**
- Reticle back-side is checked on SPARK: OK or not for NXE use ? *(see further)*
- Reticle mates with fixed EUV pod, stored in EUV pod stocker between uses on NXE
- Establishing cleaning by default before use

Reticles in use on NXE3100

- Routine back-side monitoring on SPARK interfacing via EUV pod + clean when needed *(see further)*

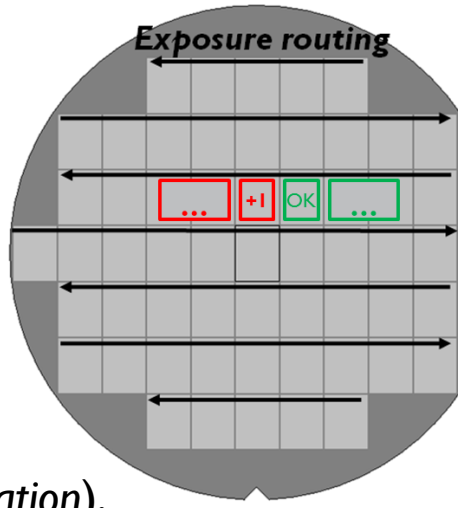
All via fully automated handling within MT *Pro* + InSync

FRONT-SIDE ADDERS ON RETICLE OVER TIME

(= PATTERN SIDE)

Specifics of way-of-working for FS adders

- Defectivity monitor in place by wafer printing.
- Particle adders monitored as new repeaters in wafer inspection results for a newly exposed wafer, compared to a previous one (reference)
- **Unloading reticle from scanner is avoided as much as possible** (kept in vacuum library of scanner in between exposures)
- Outside the scanner the reticle is in its EUV pod in the stocker, except for back-side monitoring on Süss MT-Pro (yet minimized)



Results

- **Evidence of occasional added particles during exposure and in between exposures (but inside scanner)**

Discussion

- Target for clean handling must remain 0 adders
- In parallel to continuous scanner improvement, ASML is studying feasibility of a pellicle solution (*see next presentation*), to assure no yield loss is caused by printing adders
- ***If 0 adders cannot be assured, what is a tolerable front-side adder rate ?***

COO STUDY FOR NON-0 PARTICLE ADDERS DURING EXPOSURE

- **How 0.000000000000.... should the FS particle adder rate be ?**
  Is production possible > 0 (as integer value) ?
  - As example, is 1 adder per 10000 exposed wafers good enough ?
    This means that particles per wafer (PpW) = 0.0001on average
- Actually NO, **unless the time that it happens is known (better).**
  Otherwise usable yield is not known (and cannot be confirmed >0)
- **Intermediate solution: frequently check reticle**
- How to detect an adder?
  - Wafer inspection + repeater analysis: in principle not sensitive enough
    + not optimum for all possible mask patterns
  - Patterned mask inspection: expected to detect all that would print
- **How frequent to check (+ clean if required) ?**
  - Can PMI @wafer fab be a cost-effective solution to better determine the time of the adder ?
  - Idea:
    - For the example given: expose 1000 wafers, then the chance of adder is 10%.
      Next reconfirm reticle after every1000 wafers by PMI and clean if adders.
      Expose next 1000 wafers, etc. → **Yield loss can be imited.**
  - **Invitation to IDM's / (present and future) NXE customers :**
    please provide feedback,
    and upon follow-up request also cost center input for COO work-out.

BACK-SIDE DETECTIONS OF NXE RETICLE
(= CLAMP SIDE)

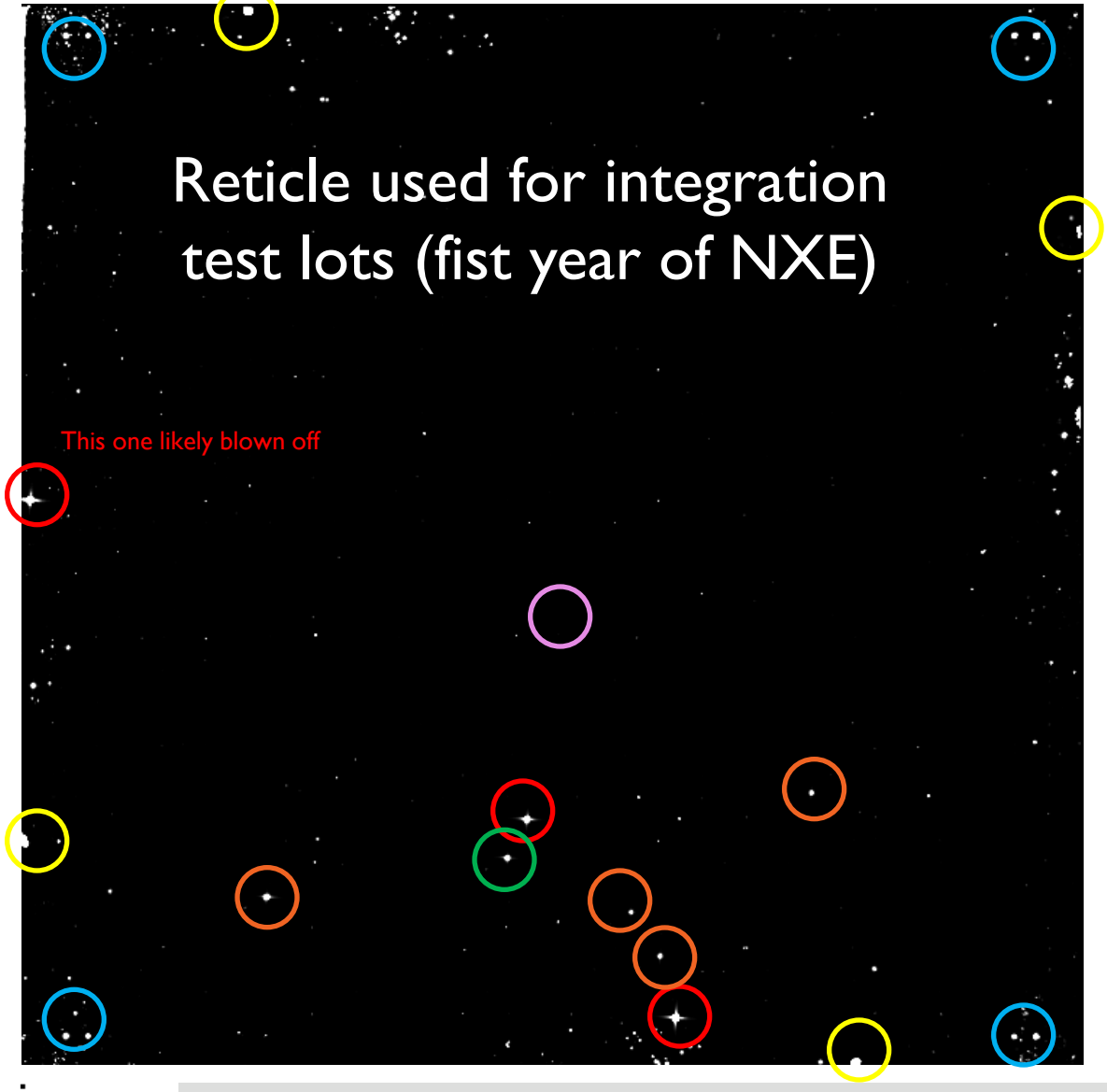
Specifics of way-of-working for BS adders

- NXE reticles are checked by SPARK for back-side cleanliness
  - Before allowing first use on NXE
  - Monitoring over time while in use on NXE
  - **<u>CRITERION</u>: Upon presence of ≥45µm detections a clean is required before (further) NXE use, as these are shown to give overlay excursions**

Results

- **Way-of-working is confirmed by examples**
  (see my talk @ EUVL Symposium session 2)
  - **Examined by height sensitive review on mask**
  - **Occurrences of particles on reticle clamp**
- Beyond particles:
  - also artifacts seen on the backside of a reticle after some time of use...

DETECTIONS ON BACK-SIDE OF NXE3100 RETICLES AFTER PERIOD OF USE according to **imec classification**



Detections considered OVL critical

Contact point EIP

Clamp corner pins

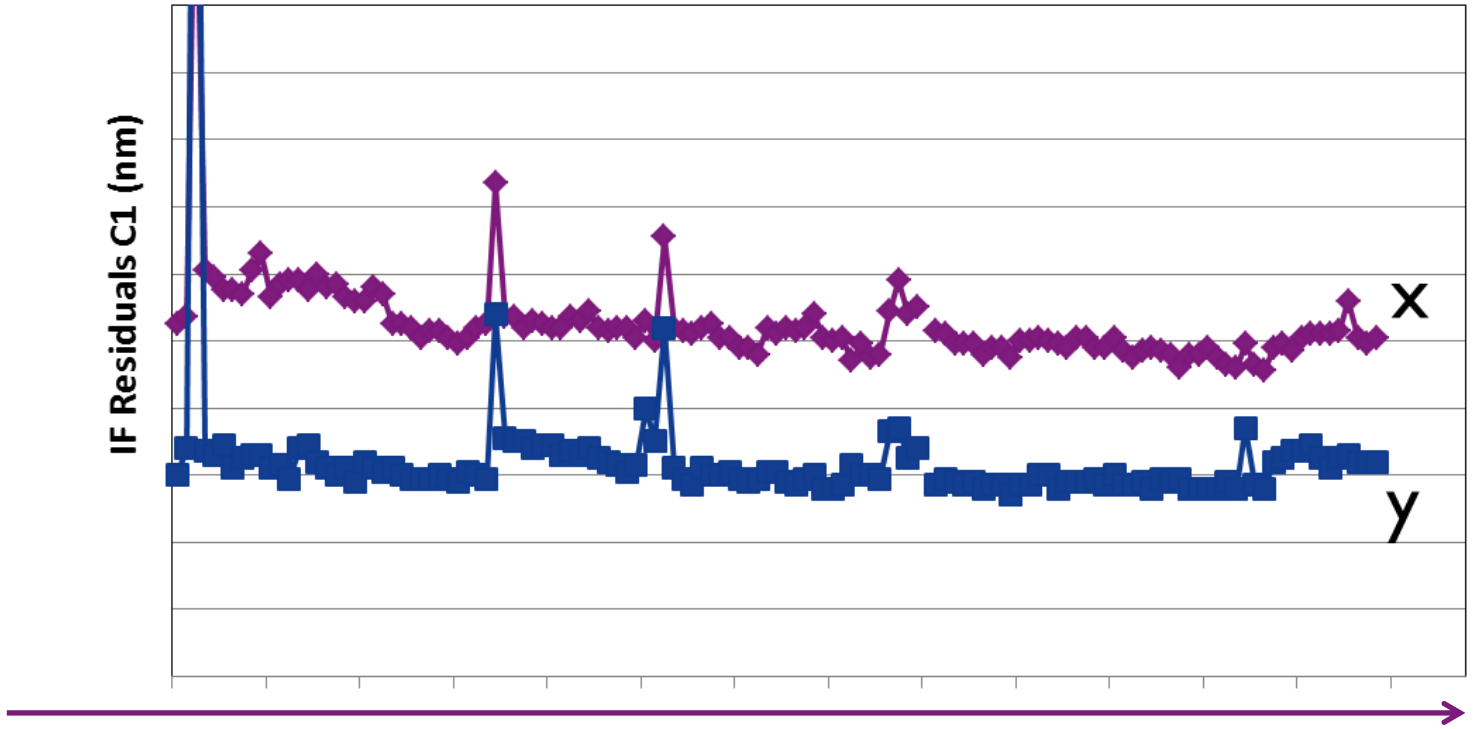
Adders since latest exposure

Detections lost over time

Historical medium-size detections (OVL un-critical ?)

WAY OF WORKING FOR BS...

... has reduced the impact and frequency of BS particles causing printed overlay excursions



Time line since NXE3100 is @imec

See Eric Hendrickx, EUVL Symp., session I

Analysis based on QA 144mm

EUV POD SHIPPING TESTS WITH BLANKS

pod type	do what
	imec-Entegris-imec
1005A in use	round trip shipment
1005A in use	round trip shipment
new 1007A	round trip shipment
new 1007A	round trip shipment
new 1007A	round trip shipment
new 1007A	ship + ISTA-3A protocol
new 1007A	ship + ISTA-3A protocol
new 1007A	ship + ISTA-3A protocol
new 1007A	control kept at imec
new 1007A	control kept at imec
new 1005A	round trip shipment
new 1005A	round trip shipment

ISTA = International Safe Transit Association

- Front-side adders: **max 3 adders** >200nm, but 1 large one near QA edge (*)
- Back-side adders: Typically largest detection is ~10µm, yet once it is >20µm (*), but **no overlay critical adder** (*)

(*) Based on SPARK, see above explanation for BS, 150nm sensitivity. For FS actually no dedicated calibration.

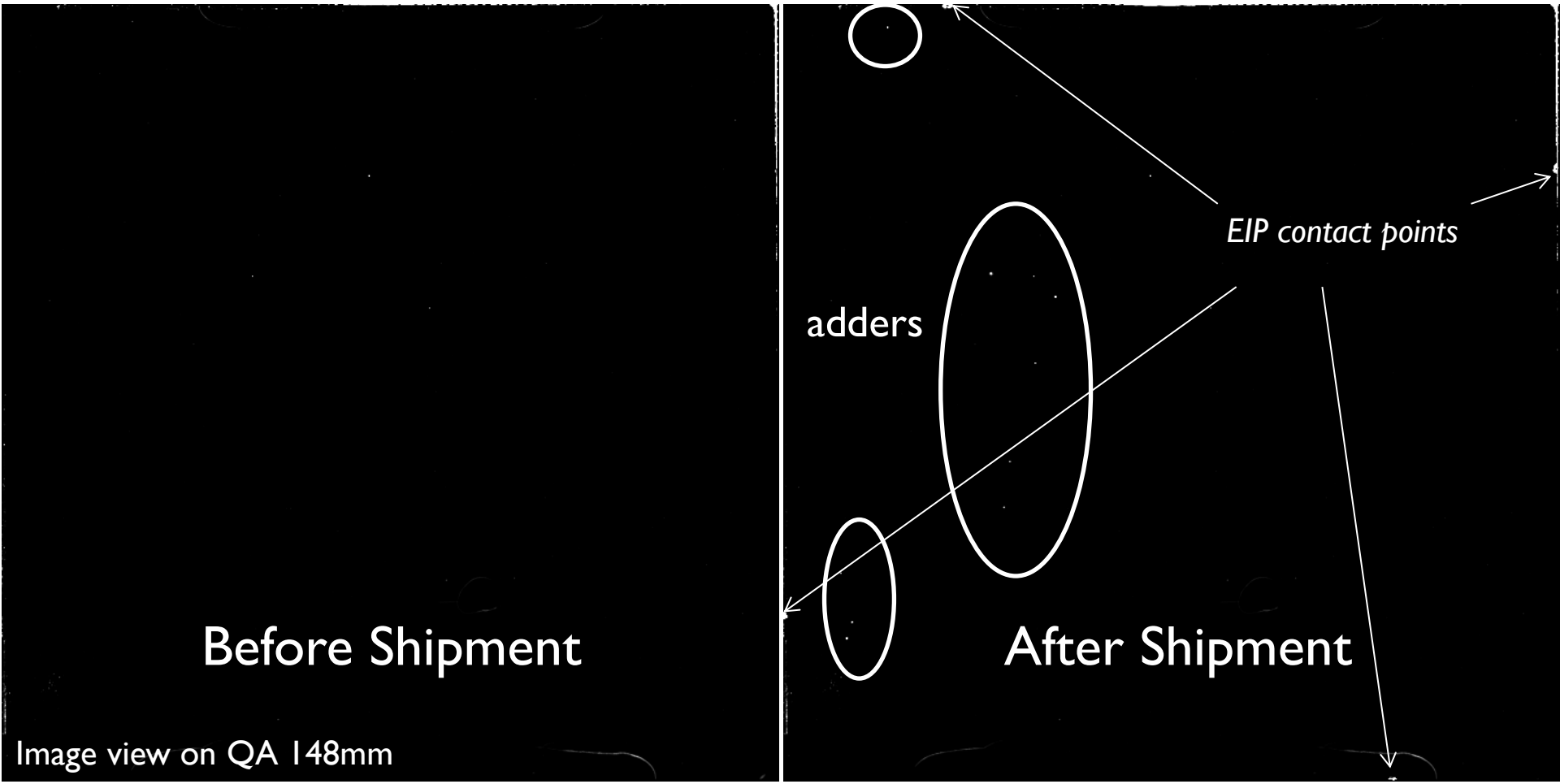
Very encouraging results → found OK to use for shipping, but recommending cleaning upon arrival to cope with few residual adders

Worst case

EUV POD SHIPPING RESULTS

pod type	do what	<---- Adders BS ------>		
	imec-Entegris-imec	>20µm	5 - 20µm	≤5µm
new 1007A	ship + ISTA-3A protocol	0	3	12

BACK-SIDE

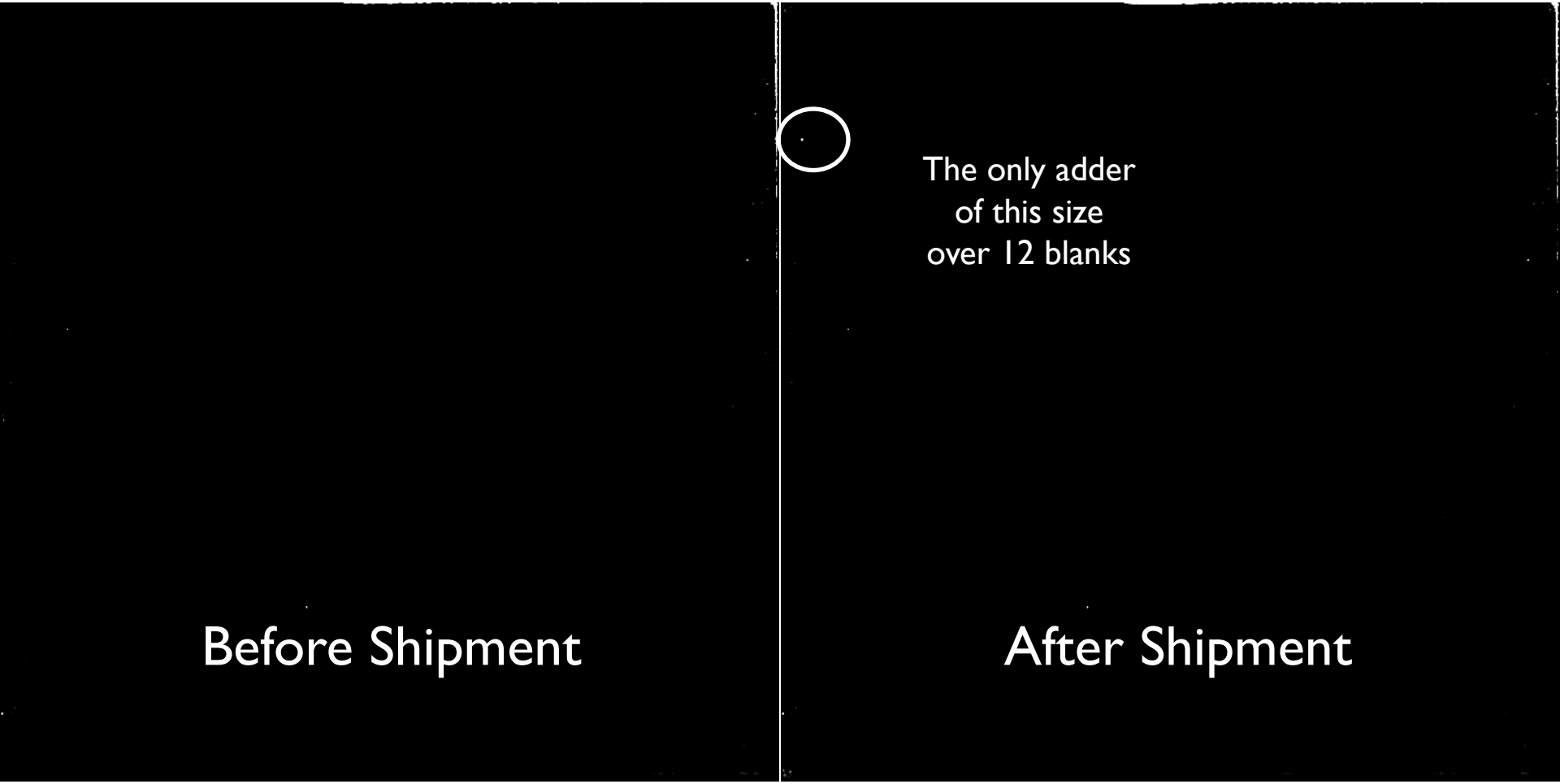


Worst case

EUV POD SHIPPING RESULTS

pod type	do what	Adders FS	
	imec-Entegris-imec	>0.5µm	<0.5µm
new 1007A	ship + ISTA-3A protocol	1	0

FRONT-SIDE



CONCLUSIONS

Shipping EUV reticles in EUV pods is **confirms expectations !**

- Back-side "just" protected by box-in-box principle
- Front-side is protected by removable hard pellicle (EIP base)

Back-side particles:

- Way-of-working successful in minimizing occurrences of particles on the reticle clamp, by flagging overlay critical particles on incoming reticles and after period of use.
- Despite avoidance of manual handling in wafer fab through interfacing with EUV pod we have occurrences of big particles after a period of use (**most of them flagged**).
- Artifacts should also get attention:
  assure they cannot give rise to printing particles on the front-side.

Front-side particles:

- **Occurrences detected**
- Yet possibly workable even if #adders is not ≡0 ? (subject for possible COO study)
- ASML makes continuous improvement in scanner to reduce probability of adders during exposure. Imec contributes by monitoring.
- *Note: the only time the EIP base does not protect the front-side is when the reticle is on the reticle stage (for exposure)*

There is a NEED & ROOM FOR IMPROVEMENT on each of the 3 aspects + an important role for CLEANING

ASPIRE
INVENT
ACHIEVE

imec

Details: see R. Jonckheere @session 2 of EUVL Symposium


New reticle arriving
Clamp corner pins
(example with untypical low-level cleanliness)
After manual reload from shipping box to RSP200
Example of partial transfer to clamp ?
Examples of first adders (subcritical)
Large detections shown overlay critical (see further)
Largest residual detection, considered OVL un-critical ⇒ can be tolerated for NXE3100 use
Examples of further adders (subcritical)