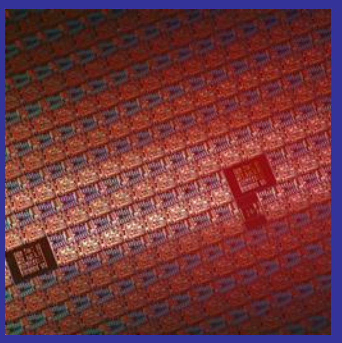
Accelerating the next technology revolution

Discussions



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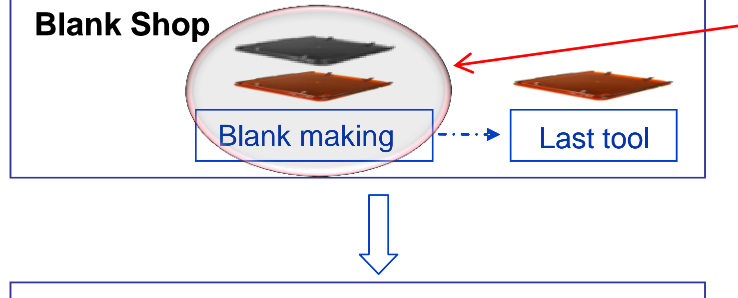
Mask Flow

Where EUV pod needed?

Blank shop:



Mask shop:

Mask Shop

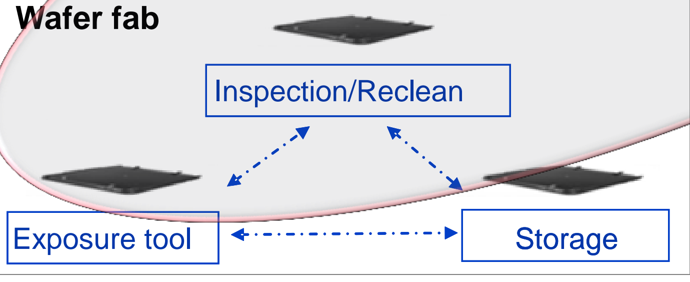
1st tool → Mask making → Last tool

-- OR --

Mask Shop

Transfer ↔ Mask making

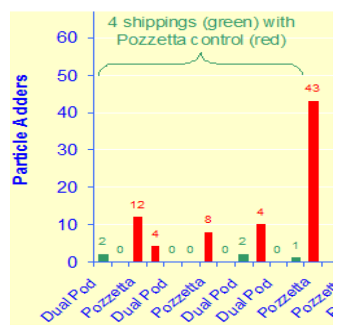
Wafer Fab:

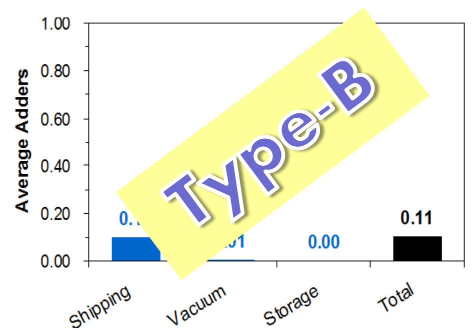


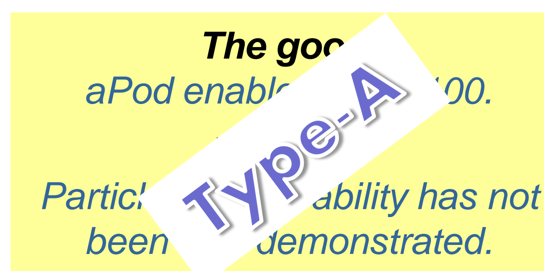
: **EUV carrier**

: **non-EUV carrier**

Key EUV Carrier Development Milestone







Dual-pod concept demonstrated

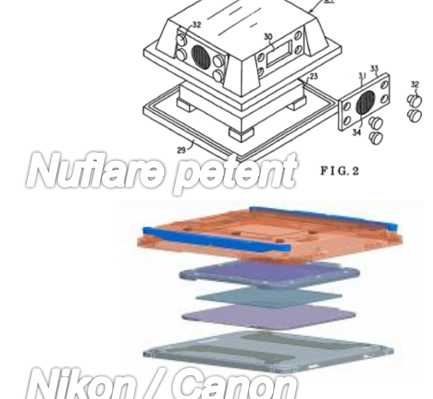
Performance capability demonstrated with sPod

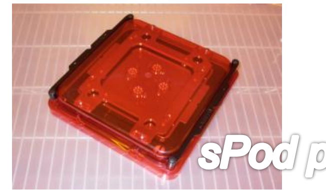
E152 EUV-pod standard established

Implementation start

200?	2007		2008		2009		2010		2011	
	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2

SEMATECH/Entegris outer-pod JDA for commercial availability of a-, n-, c-, and s-Pod.





sPod prototype

Outer pod

SEMATECH Assessment:
No Complete Carrier Solution Exists

… It requires stepped-up carrier development and steep learning!

Need	Carrier	Risk	Comment
NXE3100 tools	aPod	*(?)*	Insufficient data to conclude
***Non-exposure* tools** (clean, inspection, etc.)	aPod, sPod	*L*	Require full tool compliance with E152 standards
Shipping	aPod	*(?)*	Palletized packaging, no data
	sPod	*L*	Require *particle-free* transfer, and continuous improvements
	Clamp shell boxes	*H*	Require clean at wafer fab arrival
***In-fab* storage**	aPod, sPod	*L/M*	Need more study

Discussion Topics

1. Shipping strategy, wafer-fab mask acceptance, maskshop last tool?
2. Non-exposure tool implementation: Inspection, Clean, AIMS, Blank dep?
3. How to eliminate carrier types in E152?
4. Pod cleaning - do we have significant problems there?
5. Reticle storage - how to minimize molecular contamination?
6. ESD?
7. EUV pellicle?

Shipping

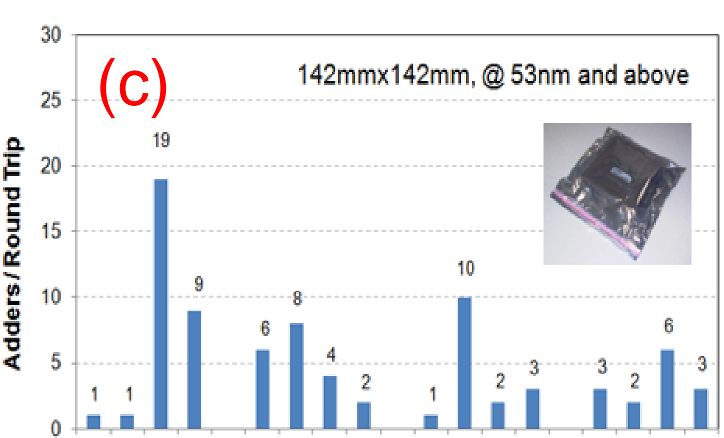
Three possible options:

(a) aPod, and Freight Services *(no data)*

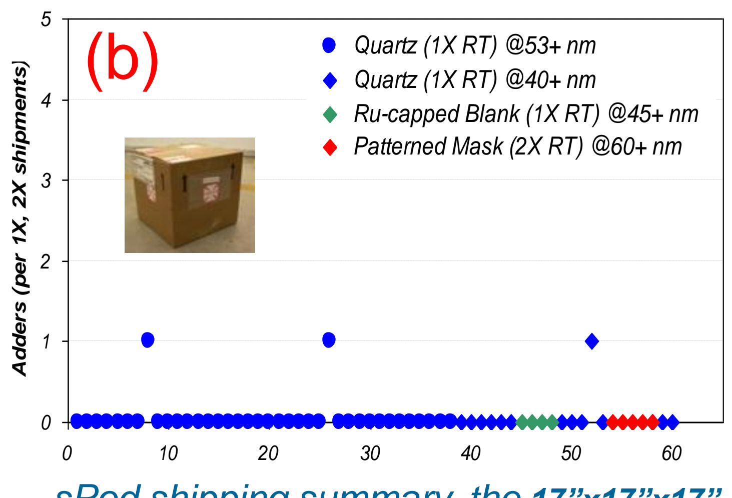
(b) sPod *(SEMATECH/Intel data)*

(c) Compact *(SEMATECH data)*

Palletized packaging for aPod, to reduce shipping shocks. It's about 12x bigger in volume than (b).



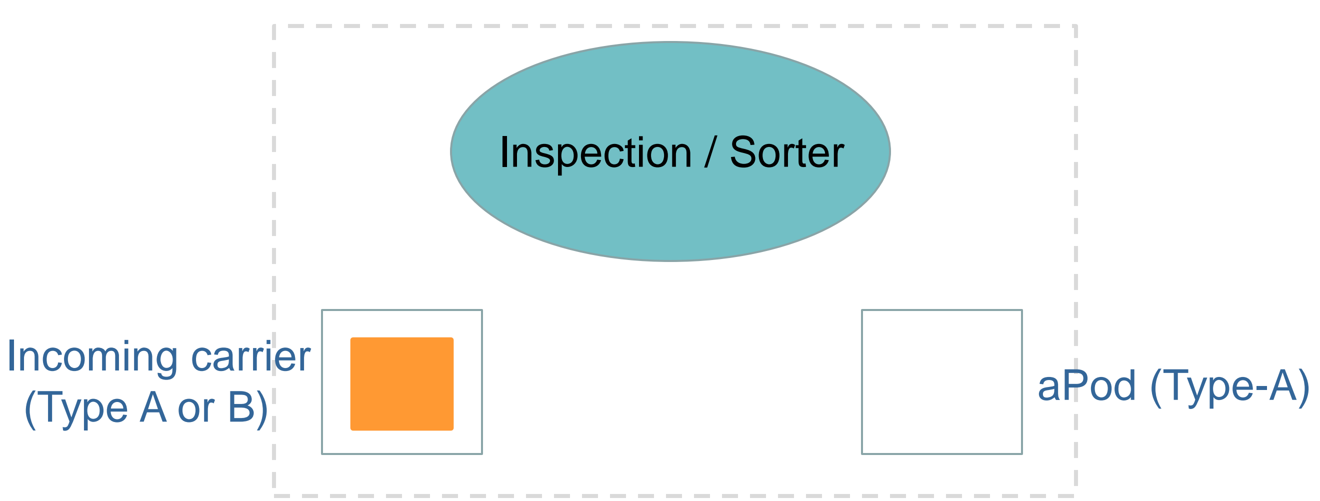
Typical shipping results with clamp shell compacts



*sPod shipping summary, the **17"x17"x17"** package is scaled to (a).*

Shipping Option / Strategy Discussion

- **What's wafer-fabs' expectation when mask arrives?** *(Is particle-free required?)*
- **Compact carrier: re-clean required at arrival**
- **aPod shipping: show capability first**
- **sPod (Type-B) shipping: no additional transfer if inspect at arrival** *(occasionally, there are particles!)*



Non-Exposure Tool Implementation of EUV pod

- **In wafer fabs**
  - All EUV mask tools such as inspection, clean, storage systems
- **In mask shops**
  - Last tool: Final clean, inspection, or reticle sorter?
  - What about AIMS?
- **How to simplify the complication of two carrier types?**
  - Implement the two specifications as discussed earlier: mask placement accuracy (within the 152.5x152.5 square) and side-wall grapping!

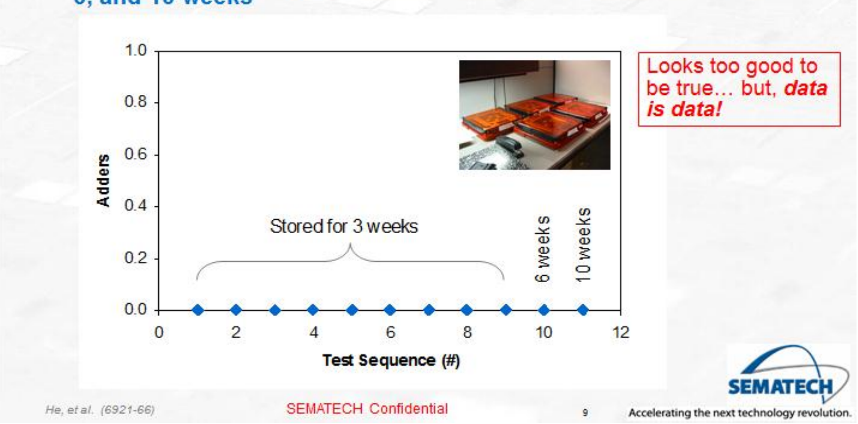
Let's Talk About How To Eliminate Multiple Carrier Types in E152 Standard

- **For wafer fabs, mask shops, and anywhere in between**
  - We must show such an able carrier exists.
  - Through E152 spec improvements before such an carrier is established. Specifically how?
  - Other options?
- **In blank shops, sPod is the best candidate at this point.**
  - EUV-pod may never need to come out of blank shops when implemented.

Storage

Key questions to answer:

- **Particulate contamination**
  - When purged
  - In static ambient environment
- **Molecular contamination**
  - "After-clean" surface
  - During shipping
  - In vacuum
  - In-fab storage
  - Carrier material outgassing



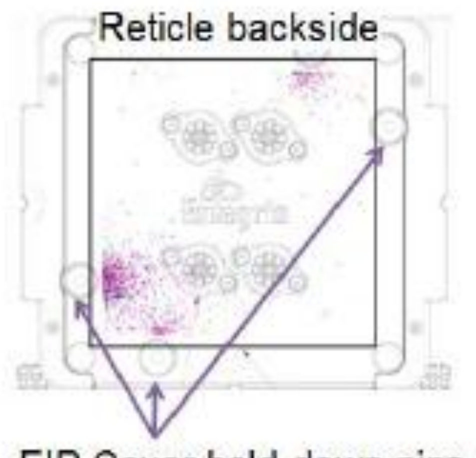
- Those tests answered the particle question while masks were un-purged, but not while purged.
- It does not say anything about molecular contamination.

BACKUP

Tests Show Earlier aPod Damages Mask When Secured like sPod in both *z-Dir* and *x-y Plane*

- The latest aPod secures mask in *z*-direction and relies on friction in *x-y* plane. ***So chamber damage no longer occurs.***
- But, need to demonstrate if the friction is enough to hold mask in place.

- NXE testing shows particles >1μm on reticle backside in location of hold down pins in the EIP cover
- Reticle damage found on chamfer edge in testing in-house pods
- It is not known why testing done earlier this year on an external test rig did not show this problem
  - Recent external testing shows similar problem in area of the hold down pin



EIP Cover hold-down pins (4)
These are pressed by 4 pins in the EUV-pod outer cover when the outer cover is latched

Damage in hold down pin area in reticle chamfer

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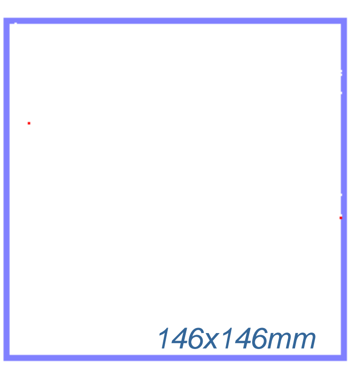
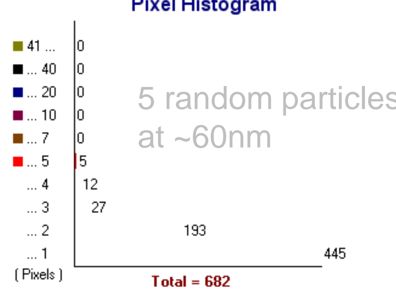




When mask secured in both z-dir and x-y plane as sPod does, aPod damages mask chamfers and causes >1um particles.

sPod showed no backside particles generated >60nm after 60x manual, worse case open-close tests. (SEMATECH data)

Showing Type A could be effectively running “in Type-B mode” when mask is placed within the tighter, Type B mask positioning spec.

153.1x153.1

152.5x152.5

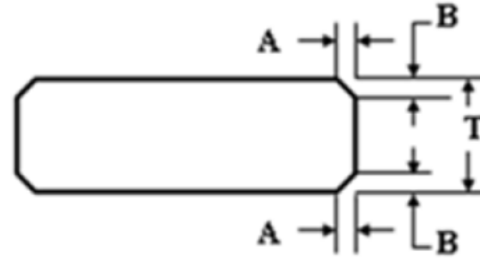
0.3mm

Mask

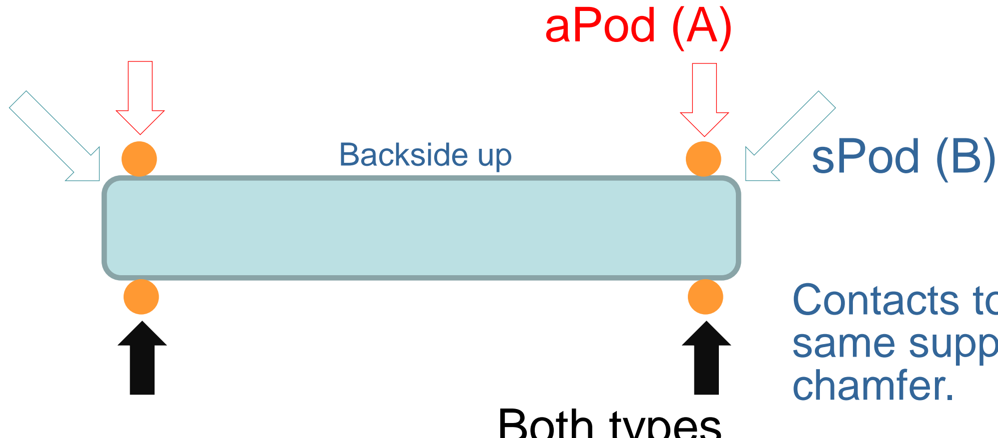
Concept of Mask Securing in EUV carriers

Basic requirements:

- Provide sufficient mask supports in both x-y plane and z-direction, and
- Without particle impact



Substrate x-section. P37 specifies edge chamfers by A/B 0.2 ~ 0.6 mm. (P37 Figure 3)



Contacts to mask in EUV pod. Type A/B share same supports on front side, differ in backside or on chamfer.