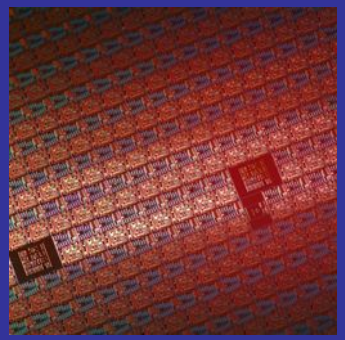
Accelerating the next technology revolution

Defectivity Budget



David Chan / George Huang

October, 2009

EUV Mask Defectivity Sheet

- Objective:
  - Set goals for pilot line and HVM
  - Assess current defective level and assess gaps from goals
  - ID critical steps to direct industry invest resources in mitigation
- Team
  - SMT: Sean Huh (SEC), George Huang (UMC), Patrick Kearney, Abbas Rastegar, David Chan
  - Survey companies
    - SEMATECH Project Leaders
    - Semiconductor Users
    - Mask House
    - Material Suppliers

Approach

- All numbers presented are ~50 to ~70nm. Better inspection tool capability is available but not very common.
- Not all data submitted are statistically valid but have good indications on level of defectivity.
- Does not have sufficient amount of known data showing favorable trade off between defect removed and add
  - Deposition smoothing technique for substrate and ML
  - Blank defect repair
- Substrate smoothing changes aspect ratio. No sufficient data on printability reduction from smoothing.
- Printability data based on limited data. Focus to be on both size and height. Need refinements.
- Survey as many companies as possible.

First Inputs

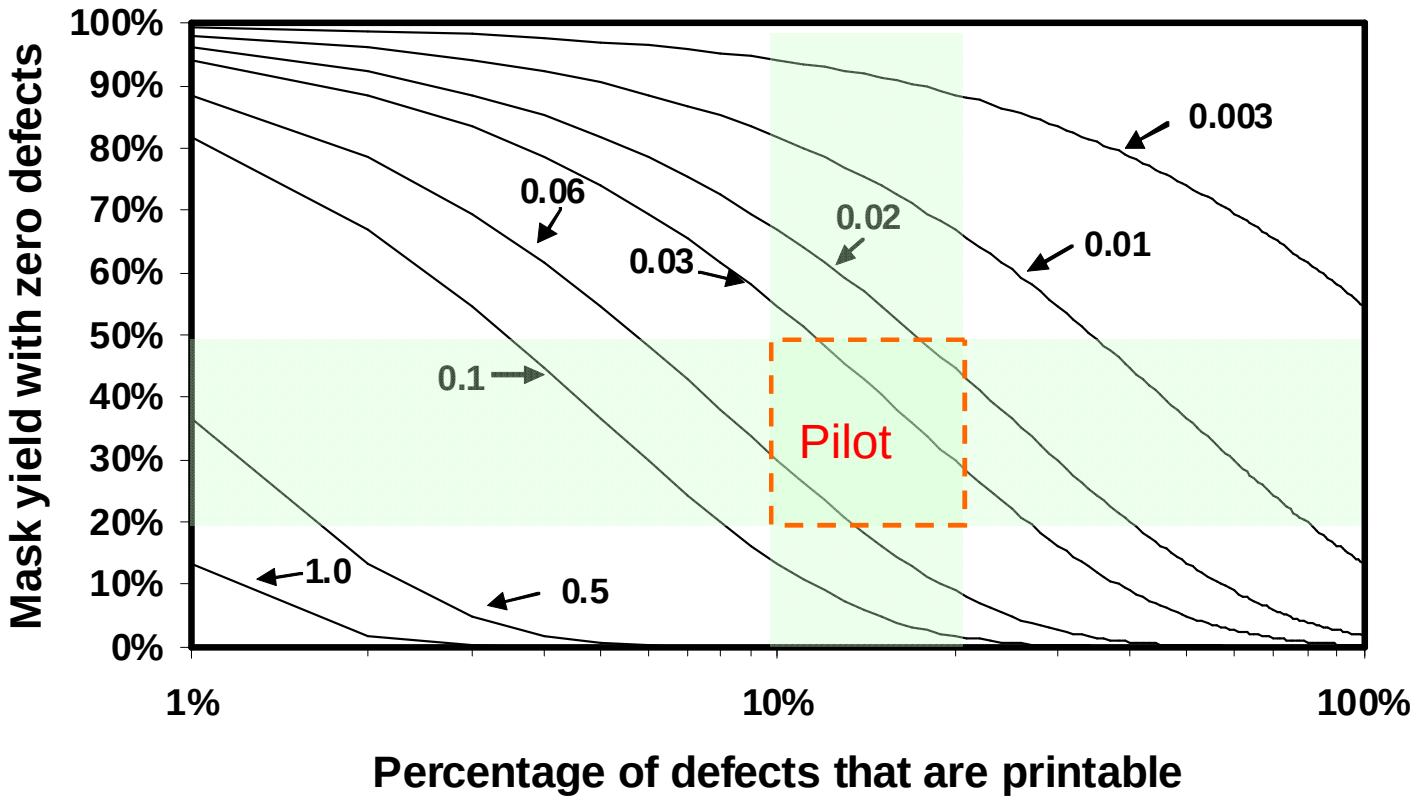
#	Process Step	Pit Type Defects Survey Results			Particle Type Defects Survey Results			All Defects Survey Results		
		n	High	Low	n	High	Low	n	High	Low
1	Substrate Manufacture									
2	Substrate Cleans									
3	Substrate Cleans Smoothing									
4	Substrate Deposition Smoothing									
5	ML-Deposition									
6	Cap-Layer Deposition									
7	Cap-Layer Cleans									
8	Mask Blank Defect Repair									
9	Absorber Deposition									
10	Pattern Placement Defect Mitigation									
11	Resist Process									
12	Pattern Etch									
13	Patterned Cleans									
14	Patterned Defect Repair (incl. Absorber)									
	Total Defects	**3**	**10***	**3****	**4**	**125***	**15****	**4**	**135***	**18****

*** ~70nm Size**
**** 53nm Size**

Printability:

- PIT Type: 10% to 40%
- Particle Type: 25% to 70%

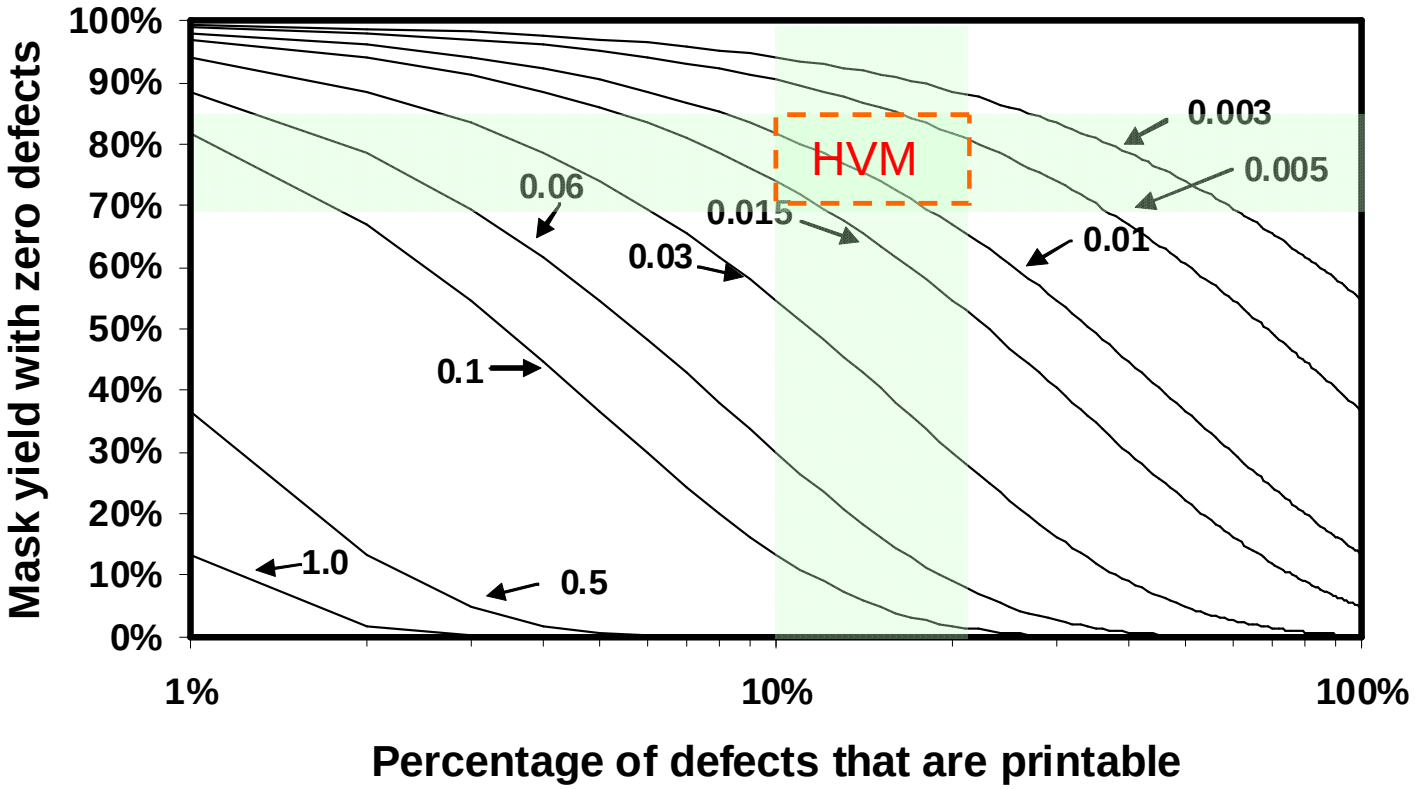
Realistic Pilot Line Defect Spec



* Graph – Courtesy from Stefan Wurm

- With 10-20% of defects resulting in printable defects (AMD results) and an initial pilot line mask yield range from 20-50% the plot line defect specification range is between 0.02 and 0.06 defects/cm^2 (0.04 mid-point).

Realistic HVM Line Defect Spec



* Graph – Courtesy from Stefan Wurm

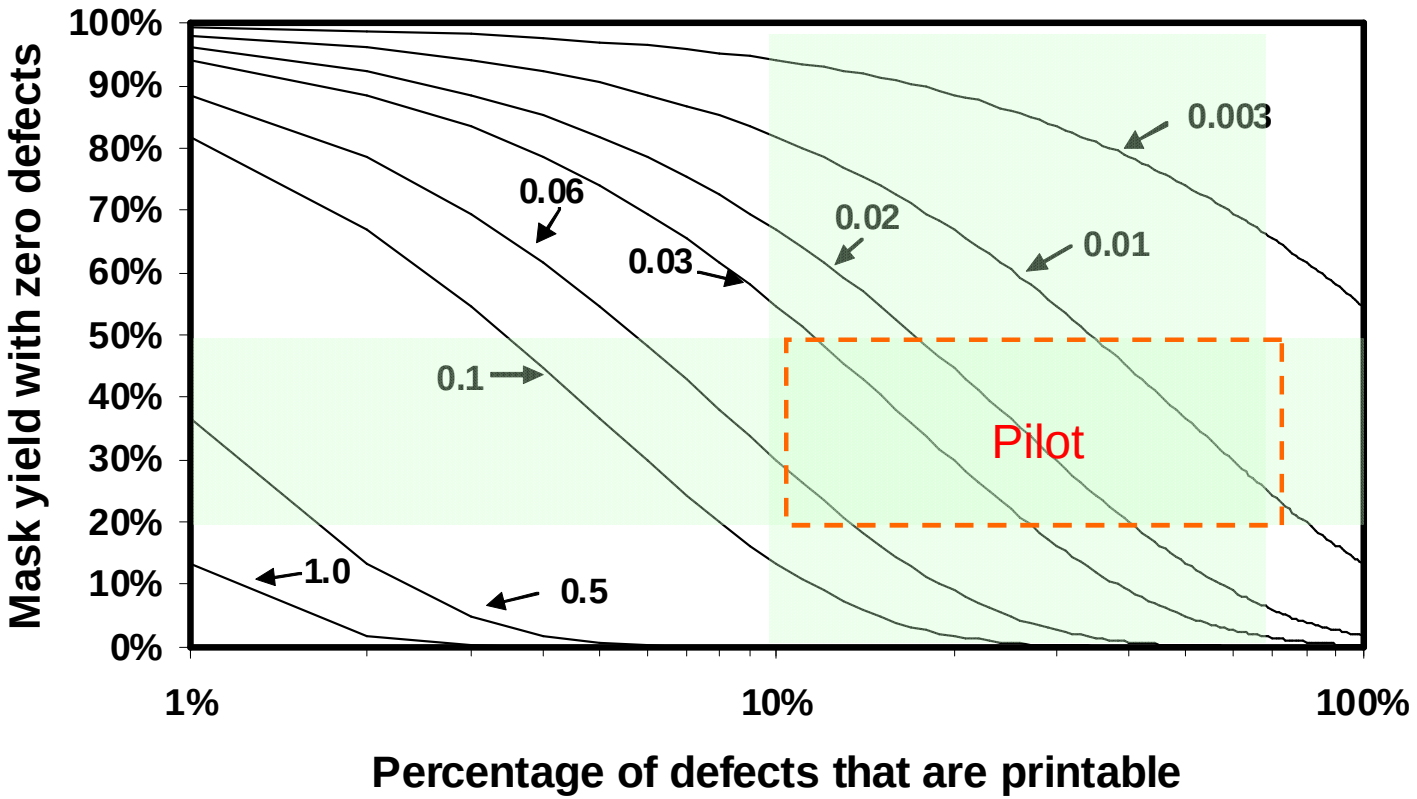
- Mask shops don't share yield data but 70-85% yield looks like a good estimate mask shops likely would be happy with. This makes a defect level of ~0.005-0.015 defects/cm^2 a realistic target area with a mid point of 0.01 defects/cm^2.

Gap Analysis – 10-20% Printability

	53nm	45nm	25nm	18nm
Current Assessment	18	29.6	177	480
Pilot Line Goal		1.51	8.1	22.0
HVM Goal		0.14		2

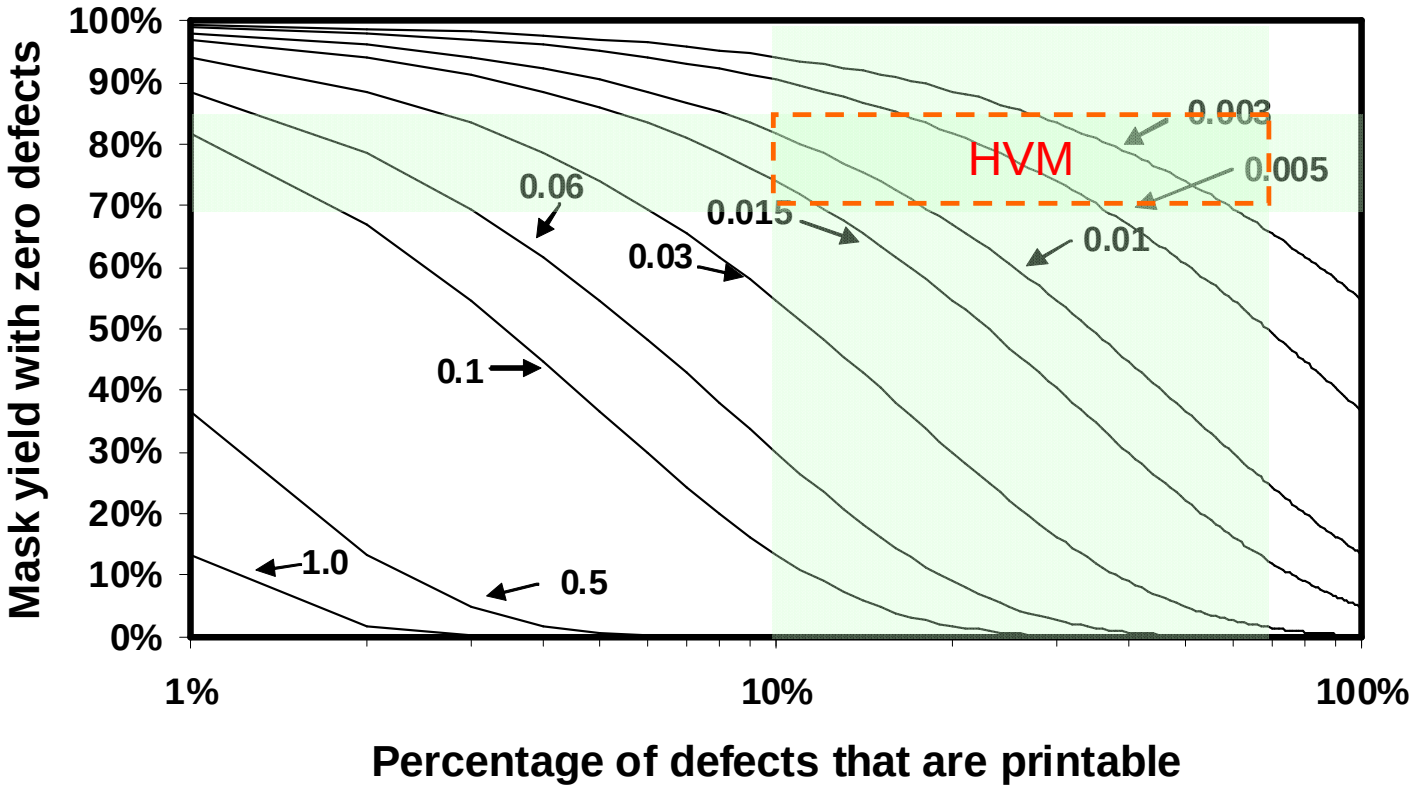
- Based on Best of Breed Analysis
  - ~25X improvement needed to pilot line in 2011
  - ~10X improvement from pilot line to HVM in 2013

Realistic Pilot Line Defect Spec



- With 10-70% of defects resulting in printable defects and an initial pilot line mask yield range from 20-50% the plot line defect specification range is between 0.01 and 0.03 defects/cm^2 (0.02 mid point).

Realistic HVM Line Defect Spec



- Mask shops don't share yield data but 70-85% yield looks like a good estimate mask shops likely would be happy with. This makes a defect level of ~0.003-0.01 defects/cm^2 a realistic target area with a mid point of 0.005 defects/cm^2.

Gap Analysis – 10-70% Printability

	53nm	45nm	25nm	18nm
Current Assessment	18	29.6	177	480
Pilot Line Goal		1.51	4.0	10.9
HVM Goal		0.14		1.0

- Based on Best of Breed Analysis
  - ~50X improvement needed to pilot line in 2011
  - ~10X improvement from pilot line to HVM in 2013

Focus Steps for Continuous Improvements

- Continue focus in ML deposition. Absorber related particle problem needs focus.
- Resist and pattern definition defect levels are crucial. Printability tends to be high.
- PIT Mitigation technique is not mature enough to rid problem.
  - Flatness compensation; loosen flatness, less CMP / PITs
  - PIT smoothing techniques
- Fiducial marking is critical to minimize impacts
- More complete printability characterization – both size and aspect ratio.
  - Simulation shows height ≤1.5nm significantly reduce printability. Push % printability ≤ 10% by height reduction.
  - Substrate/ML smoothing techniques
  - Impact from particle of 1st layer versus 40th layer should be different (any process optimization tricks? Target “conditioning”?)
- Pilot line and HVM mask defect goal needed to be refined.