IEUVI Panel Discussion

“Defect Printability Mask Standardization - Attributes and Possibility”

Semiconductor Leading Edge Technologies, Inc.

Outline

1) What specific problems we want to address in the printability study?
2) What attributes of the test blanks and masks should be addressed?

   E.g. size, shape, height, locations within stack, locations relative to device features
3) What metrology or techniques are needed to support defect characterization?
4) The pros and cons of PDM versus native defects
5) What test patterns could be used for pattern defect mask printability?

1) What specific problems we want to address in the printability study?

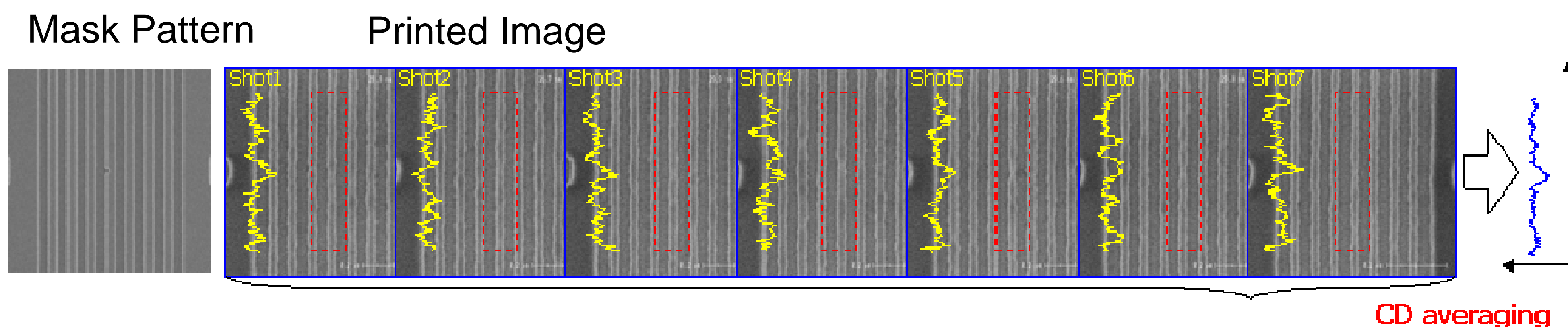
How to define the critical defect sizes.

Calculation : 3D, optical images, resist profile.

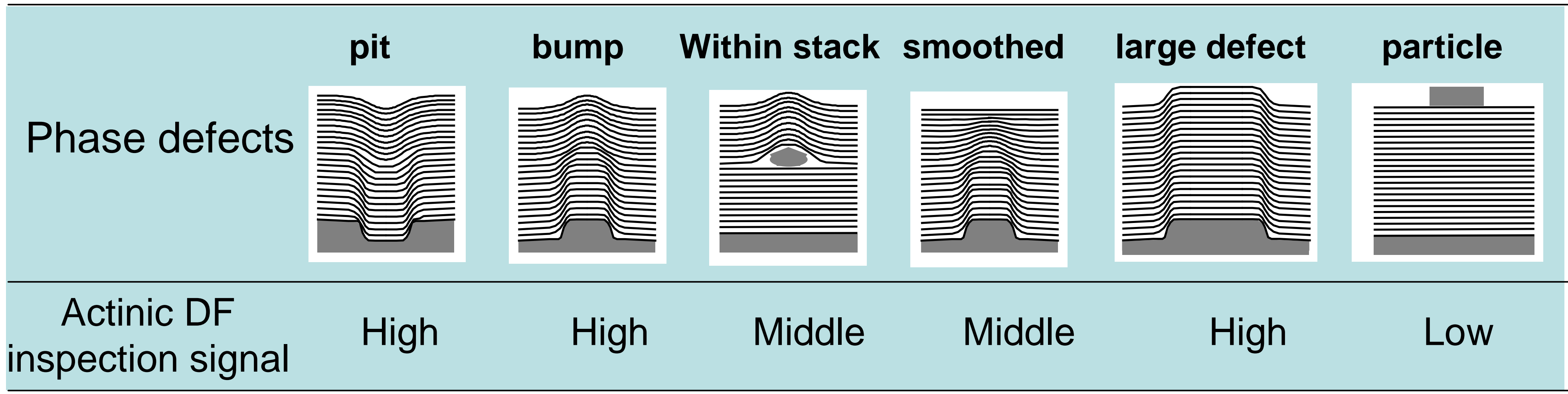
Experiments: Actual tool condition (NA, illumination σ, flare, etc.)

Making clear distinction between LER of printed resist patterns and their ΔCD induced by mask/blank defects.

→ **"Multiple-Shot CD averaging analysis"**



2. What attributes of the test blanks and masks should be addressed?



	pit	bump	Within stack	smoothed	large defect	particle
Phase defects						
Actinic DF inspection signal	High	High	Middle	Middle	High	Low

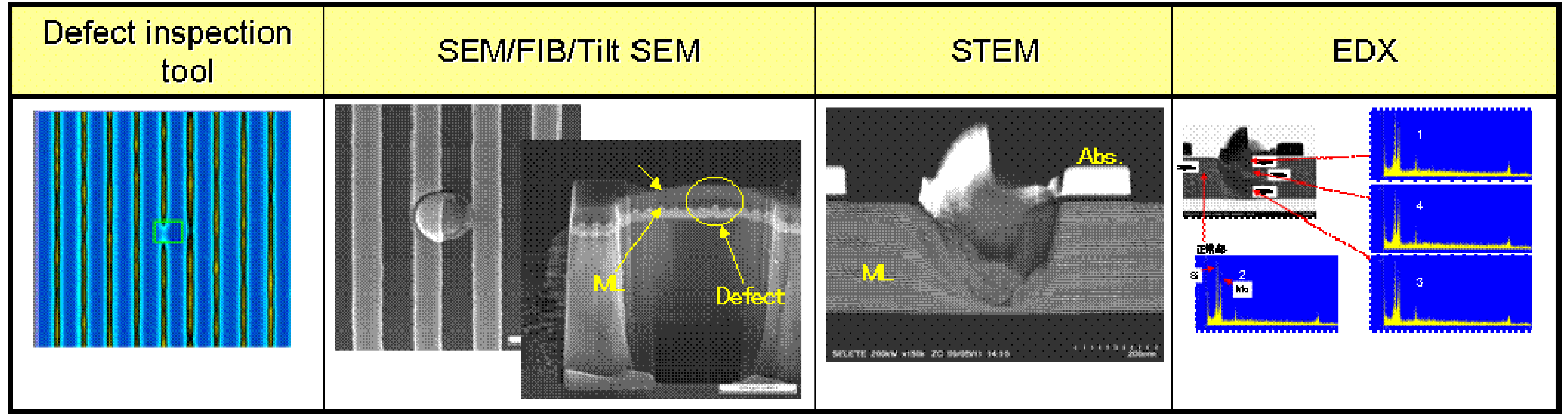
Priority of defect shape will be determined with actinic inspection results and characterization.

<u>Parameters</u>

- Height or Depth
- Width (FWHM)

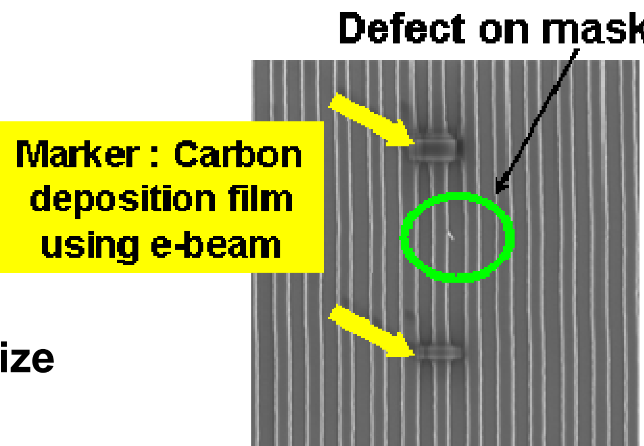
3. What metrology or technique are needed to support defect characterization?

✓ Defect inspection tool, SEM, AFM, FIB tool, STEM, EDX tool are needed.



✓ Positioning of natural defects is important to support defect characterization.

- Mask stage accuracy : SEM, AFM, FIB
- Fiducial mark is needed.
- Mark on mask to define printed defect position on wafer.



✓ Simulation

- High speed and high precision simulator for the smaller size

4. The pros and cons of PDM versus native defects

	Pros	Cons
PDM	•Useful to evaluate inspection sensitivity due to the clear definition of size, shape, and location.	•Not all types of defects can be emulated. •Difficult to fabricate, especially small phase defects.
Native defects	•Possible to evaluate real defects. •Support real mask/blank yield enhancement.	•Hard to evaluate inspection sensitivity. •Suppliers not willing to disclose.

5) What test patterns could be used for pattern defect mask printability?

✓ Selete (Consortium):

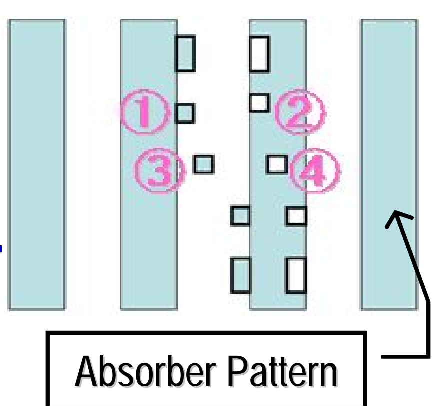
■Basic patterns and programmed typical defect modes for readiness of mask infra-structures (inspection tool / repair tool),

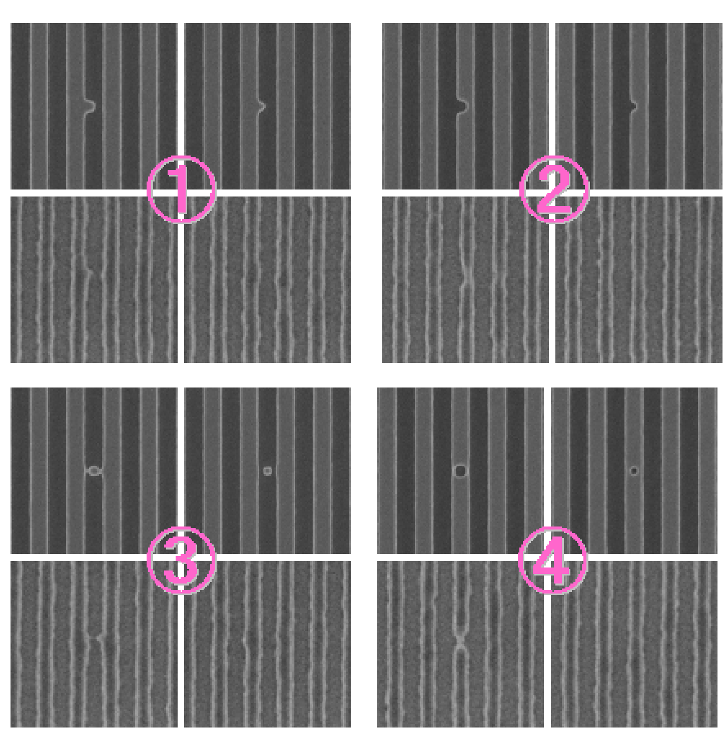
《test patterns》

L/S, C/H, Iso-Line, Iso-Hole, etc.

《test defect modes》

Pin, Dot, Intrusion, Protrusion, etc.





✓ Clients (Chip maker):

■Their own circuits patterns related to their chip products (FLASH, DRAM, Logic, etc.) , and/or their home-made, original/traditional test patterns which are competitive and not disclosed.

Defect Printability Dependence on Mask CD MTT

Isolated / Edge

Clear

Isolated

Line Width [nm]: 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16

Mask Line CD MTT :

Mask Line CD MTT :

Mask Line CD MTT :

Mask Line CD MTT: +/-10nm (5x)

Defect Size MTT: 0nm

Defect Size (1x) [nm]: 0, 4, 8, 12, 16, 20, 24

Edge

Line Width [nm]: 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16

Mask Line CD MTT

Mask Line CD MTT

Mask Line CD MTT

Mask Line CD MTT: +/-10nm (5x)

Defect Size MTT: 0nm

Defect Size (1x) [nm]: 0, 4, 8, 12, 16, 20, 24

Opaque

Isolated

Space Width [nm]: 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16

Mask Space CD MTT

Mask Space CD MTT

Mask Space CD MTT

Mask Space CD MTT: +/-10nm (5x)

Defect Size MTT: 0nm

Defect Size (1x) [nm]: 0, 4, 8, 12, 16, 20, 24

Edge

Space Width [nm]: 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16

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