

2009 iEUVi Mask TWG Panel Discussion topic:

# **Defect Printability Mask Standardization Attributes and Possibility**

**Ted Liang**

**Components Research  
Intel Corporation**

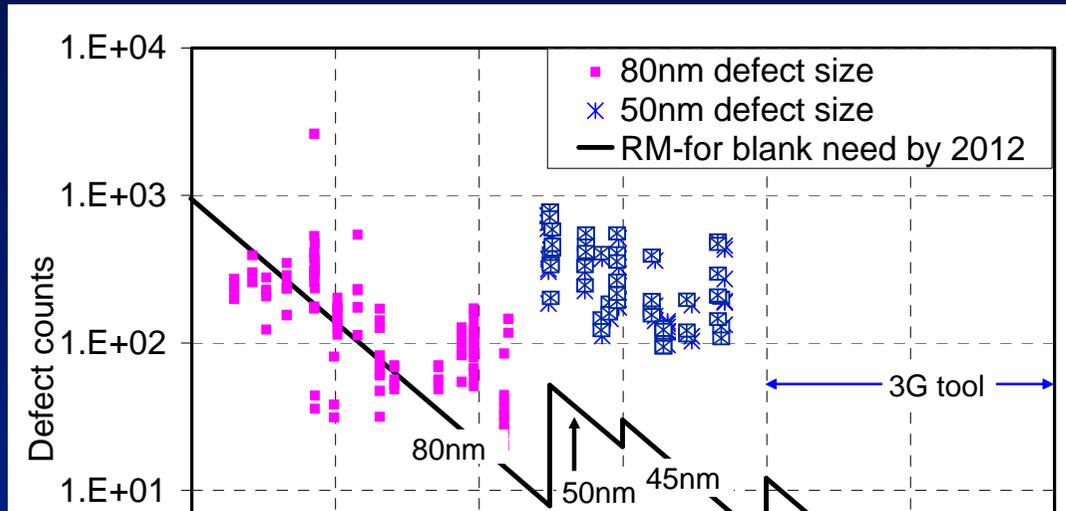
**Oct. 22, 2009**

# #1 Problem for EUV Mask

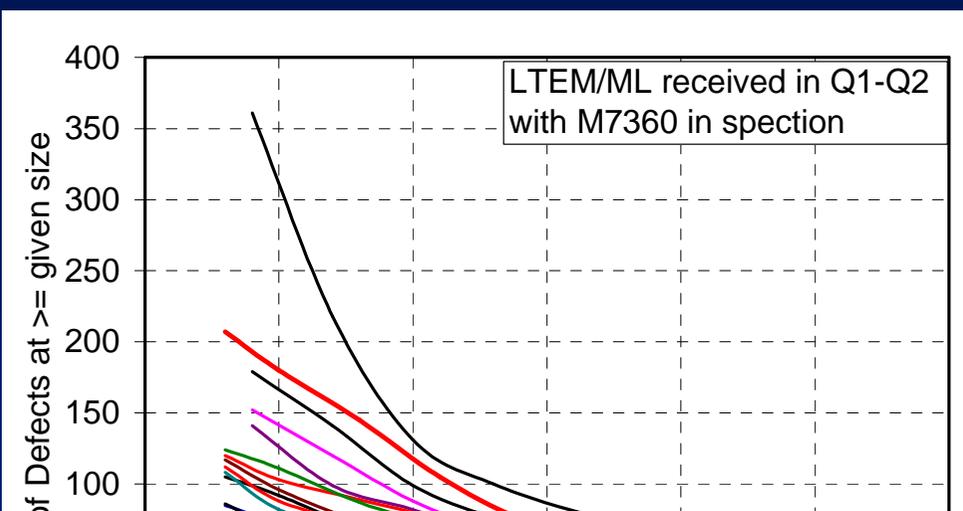
- ML blank defect is #1 problem for EUV mask
- The industry's focus should be to eliminate this problem
- The iEUVi TWG work should serve the purpose of facilitating the industry's effort in resolving the #1 problem
  - Reduce ML defect
  - Render ML defect
  - Mitigate ML defect – for example, fiducial mark

# Blank ML Defect Trend

## Total defect count



## Size distribution



**Majority of these defects detected today are printable for 22nm – 16nm hp line and space patterns**

# Ensuring Defect-free

- **Defect is a difficult 'thing' in yielding a mask**
  - Impact of defects on mask is binary – 1 defect kills the mask; there is no statistics here. Huge benefit for defect covering!
  - Impact of non-mask defects on wafer is scalar – defects kill 5% of the dies, you still can have 95% die yield
- **Defect detection must be 100% - at least this is what we want the tool suppliers to deliver**
- **Printability determines defect requirements through focus, not at best focus!!!**
  - Usually expressed in  $\% \Delta CD / CD$  as the criteria

# Standardization or not?

- **What will be facilitated by such a standard?**
  - ???
  - This should not be a SEMI standard
- **Can it be standardized?**
  - Printability is specific to device patterns
  - Users define their own defect requirements – pattern specific
  - Users select the tools that best meet their needs
- **It will be helpful, but may not be necessary**
  - Useful for benchmarking by a consortia where members can not share proprietary patterns/specs
  - For example, for inspection and imaging tools benchmarking
  - For example, for blank defects benchmarking

“ We would like to invite you as the panelists for this discussion. Each panelist is requested to present 2-4 pages on the following to stimulate discussions:

- 1) What specific problems we want to address in the printability study? **What defects print on particular patterns at certain criteria**
- 2) What attributes of the test blanks and masks should be addressed? E.g. size, shape, height, locations within stack, locations relative to device features. **All of the above**
- 3) What metrology or techniques are needed to support defect characterization? **AIMS, SEM, AFM, spatially resolved composition tool for 'native' defects**
- 4) The pros and cons of PDM versus native defects: **They serve different functions which can not be substituted with each other. PDM - simple, well characterizable, unambiguously measurable, utilized as a reference for tool development and qualification; native – reality check and yield improvement through root cause analysis which can only be done with native defects.**
- 5) What test patterns could be used for pattern defect mask printability? Availability? **Patterns relevant to device and sensitive to defects**

# Two Related Suggestions

- **Define a reference/standard for sizing ML defect: must be measurable, quantifiable by  $\% \Delta CD / CD$  in the worst printability case, available for wide use by blank suppliers, users and tool suppliers**
  - SiO<sub>2</sub> sphere-equivalent, SEVD, height x FWHM, etc
- **Replace defect density with total defect count**
  - It was originally used when defects are in 1000s – 10,000s
  - It was used for gauging blank yields for suppliers
  - Now we should transition it to serve the purpose for blank users as a figure of merit per blank: if the defect count is n/blank, can it be used? For which layer? More meaningful.
  - Defect counts per plate is generally used by the mask industry today