IEUVI Mask TWG Panel

Buried defects investigated with simulation

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65nm is the worst case surface FWHM

CD Change for 22nm lines with defect located 25nm from the shadowed absorber edge

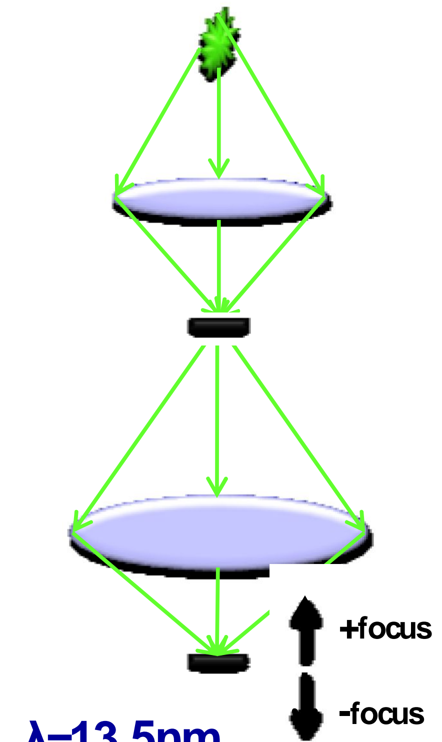
Surface Defect Height (nm): 4, 3.5, 3, 2.5, 2, 1.5, 1, 0.5

Surface Defect FWHM (nm): 20, 40, 60, 80, 100

Colour scale: 0, 5, 10, 15, 20

RADCIAL Simulations

Optical Model



λ=13.5nm

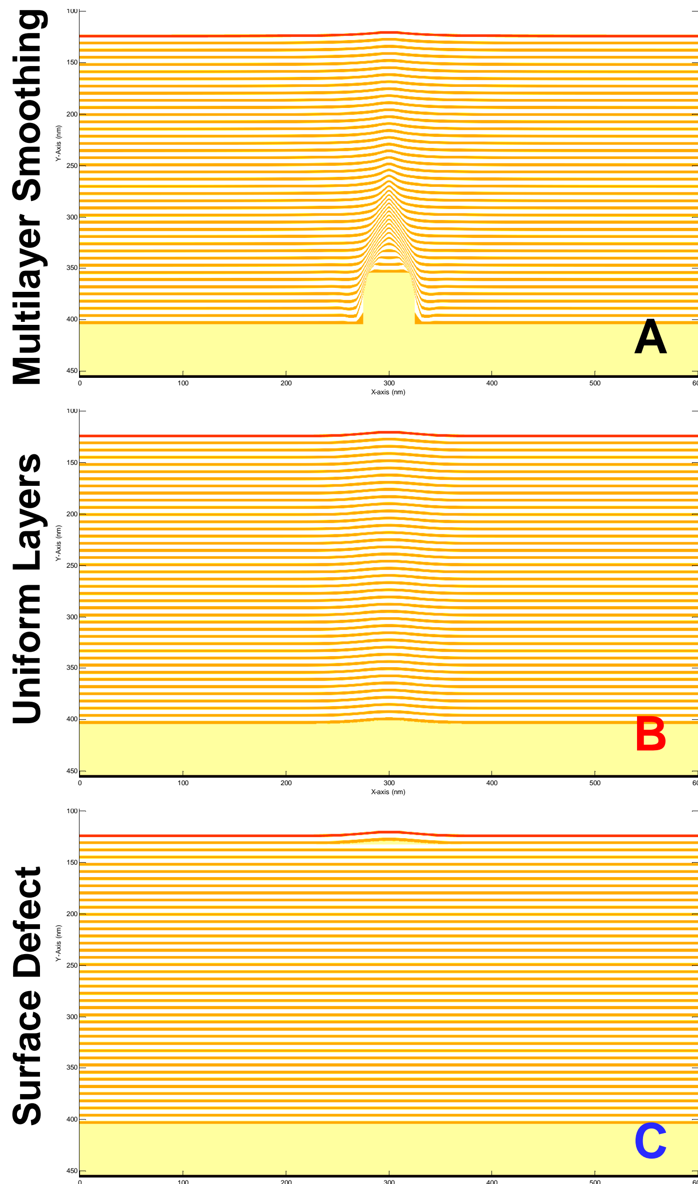
NA=0.32

4x Reduction

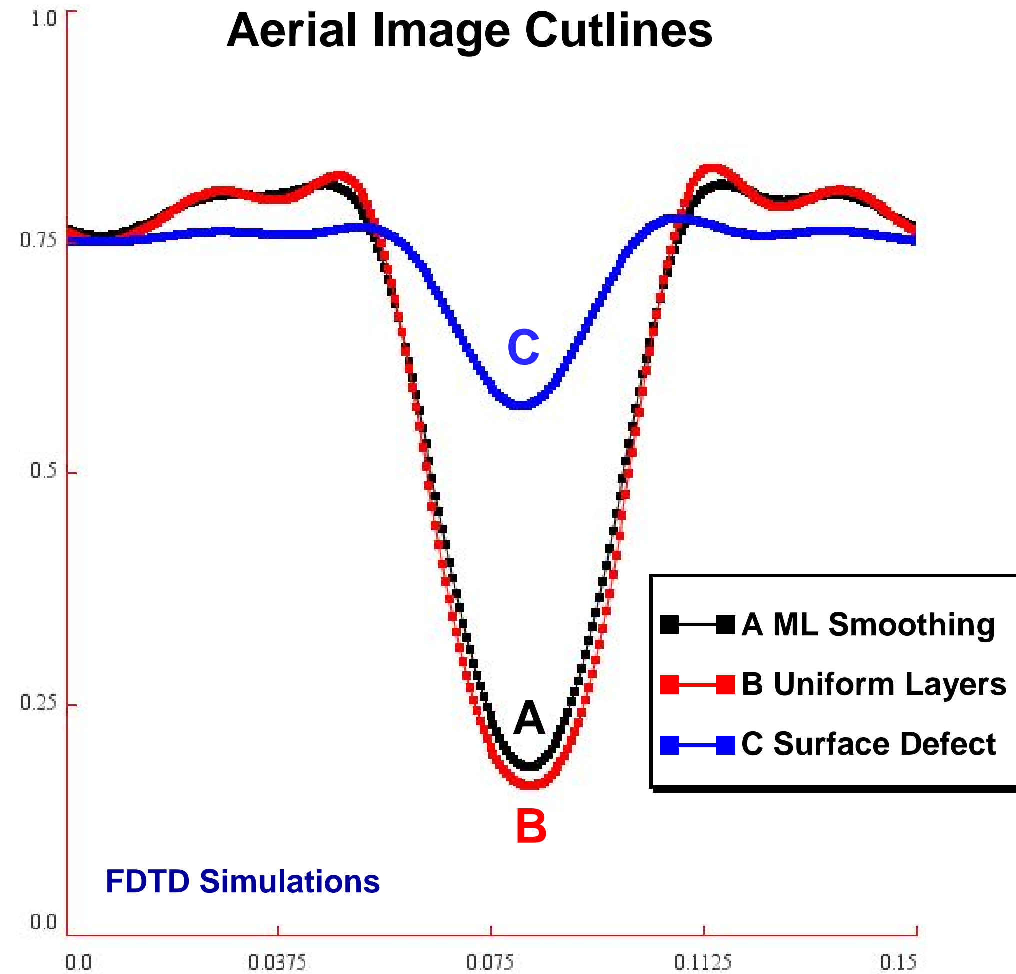
σ=0.75 Except for final section on illumination

6° incident light

What is below the multilayer surface?

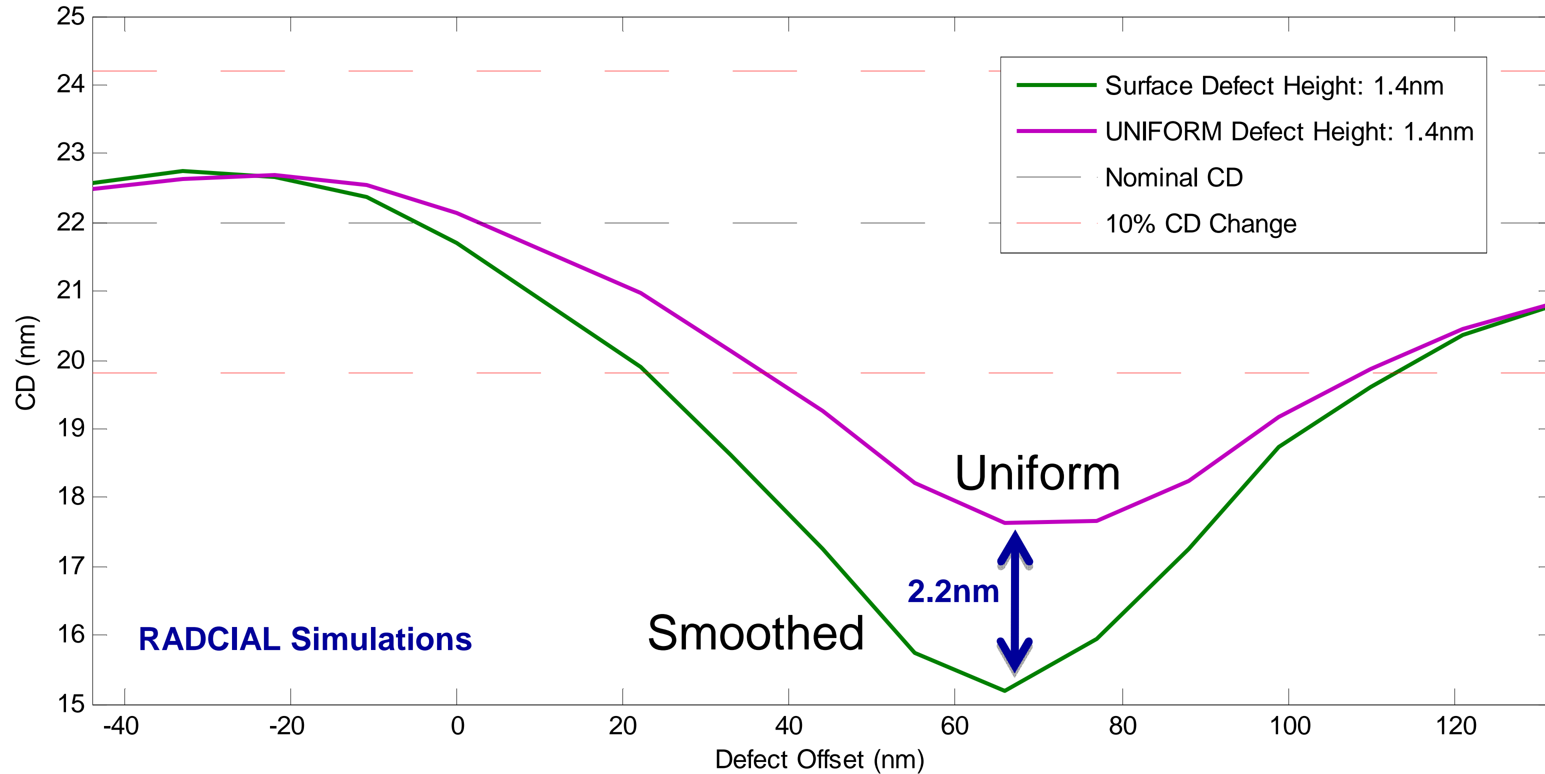


Three example geometries, all with a surface height of 3.55nm, and FWHM of 59nm (3.55nm = 189°)



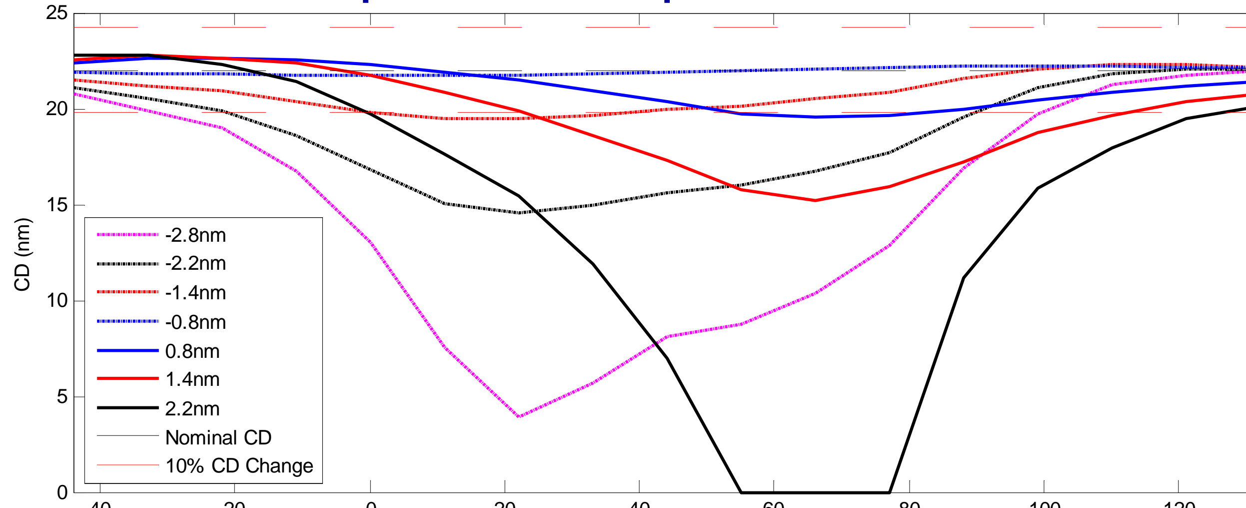
For the rest of the presentation, all multilayers are smoothed like the TOP figure unless noted otherwise

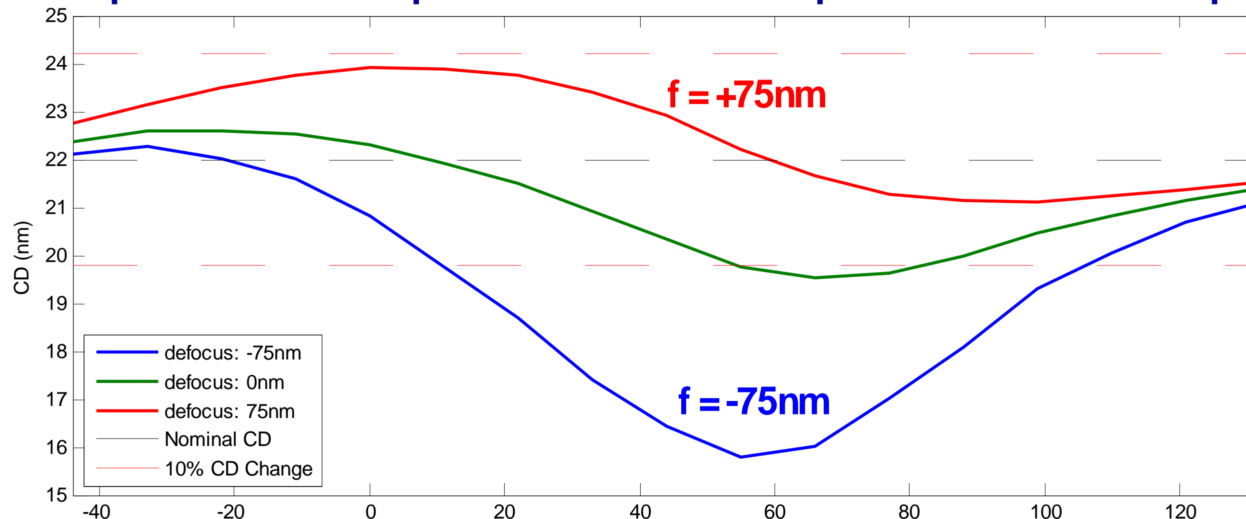
Multilayer has a larger effect for defects near features



	Surface Height	Substrate Height
Smoothed	1.4nm	5nn
Uniform	1.4nm	1.4nm

Summary of Buried Defect Printability for 22nm Dense Lines

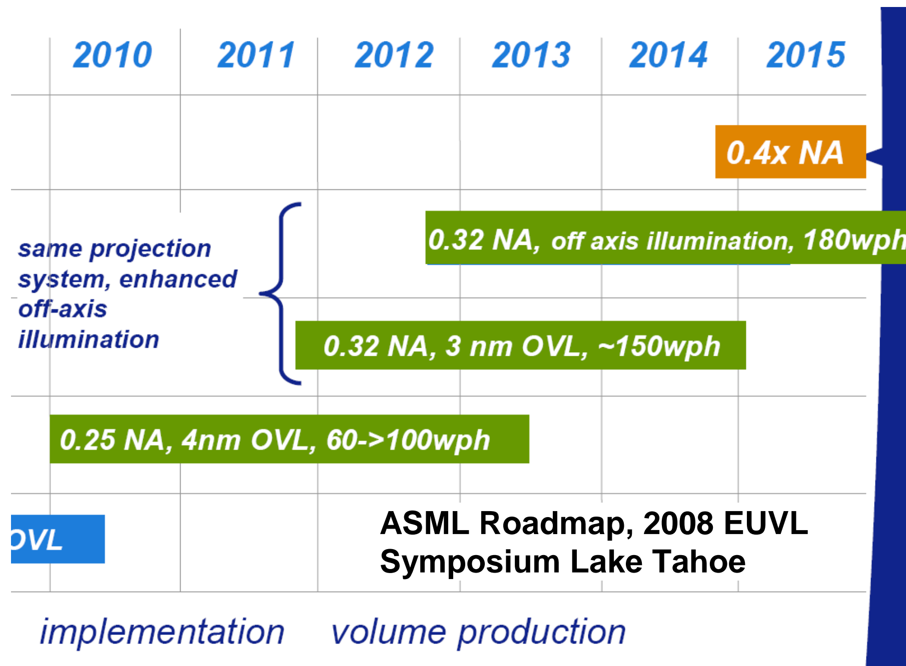




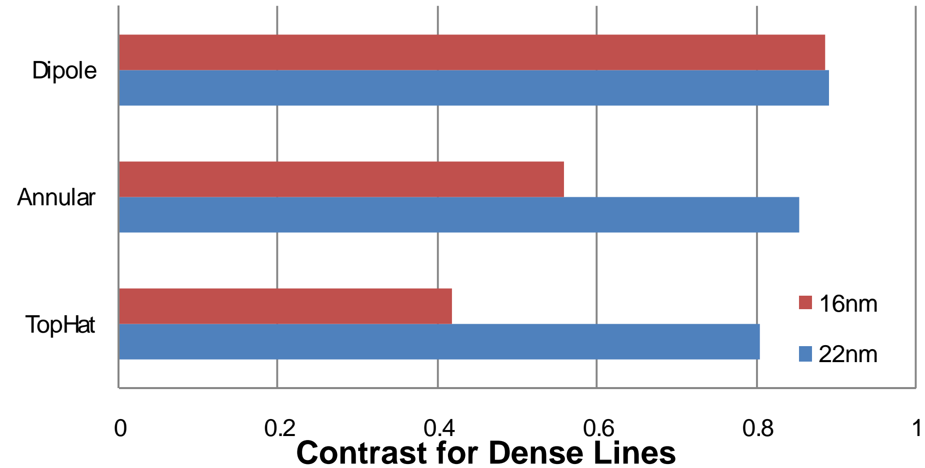
- Maximum allowable surface bump: 0.8nm
- Maximum allowable surface pit: 1.4nm
  - No ML smoothing for pits
- Pits have opposite worst case position
- I believe worst case position is determined by the relative phase related to nonzero k_x caused by 6° incident light
- Allowable defect size depends on expected focus variation
- Already verified by experiments

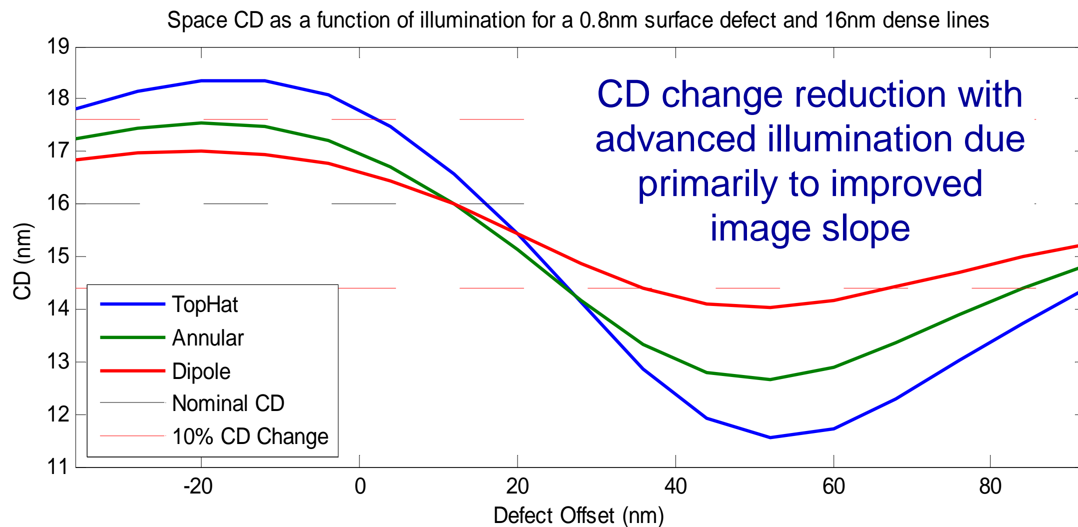
RADCIAL Simulations

Illumination Effects Defect Printability



Off-axis illumination will likely be used when HVM EUVL is introduced





Images of an isolated defects