EUV Mask Readiness:
Pilot Line 2010 - 2012
EUV Mask Readiness for Pilot Line

➢ It’s Showtime for EUVL
  - We have about 2 to 3 years to enable EUVL Pilot Lines for at least two of our member companies.
  - If EUVL fails to work in these pilot lines then the future is bleak for EUVL.

➢ We need to concentrate on high risk items
  - Resources are limited

➢ IEUVI Task:
  - Identify current high-risk ‘Will Not Be Ready’ issues facing pilot-line readiness
    - Highlight those issues where new projects could help
    - Identify work-around options where high risk is unavoidable
Survey of Mask readiness for Pilot line production

Respondents asked to rate their perception of EUV Mask Infrastructure Readiness for Pilot Line Manufacturing: 2010-2012

Key requirements from the ITRS Roadmap for EUVL Masks were included for use in judging readiness.

<table>
<thead>
<tr>
<th>ITRS REQUIREMENTS</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask Nominal Feature Size</td>
<td>120nm</td>
<td>107nm</td>
<td>95nm</td>
<td>86nm</td>
</tr>
<tr>
<td>(Nominal Feature Size at Wafer)</td>
<td>(30nm)</td>
<td>(27nm)</td>
<td>(24nm)</td>
<td>(21nm)</td>
</tr>
<tr>
<td>Mask 3σ CD uniformity MPU gates</td>
<td>2.7nm</td>
<td>2.4nm</td>
<td>2.1nm</td>
<td>1.9nm</td>
</tr>
<tr>
<td>Mask 3σ CD uniformity DRAM dense</td>
<td>5.2nm</td>
<td>4.6nm</td>
<td>4.1nm</td>
<td>3.7nm</td>
</tr>
<tr>
<td>Mask Image Placement, max error</td>
<td>5.4nm</td>
<td>4.8nm</td>
<td>4.3nm</td>
<td>3.8nm</td>
</tr>
<tr>
<td>LTEM substrate flatness peak/valley</td>
<td>51nm</td>
<td>46nm</td>
<td>41nm</td>
<td>36nm</td>
</tr>
<tr>
<td>LTEM substrate minimum defect size</td>
<td>36nm</td>
<td>33nm</td>
<td>31nm</td>
<td>30nm</td>
</tr>
<tr>
<td>Mask minimum defect size</td>
<td>40nm</td>
<td>36nm</td>
<td>32nm</td>
<td>29nm</td>
</tr>
</tbody>
</table>

Asked to classify ‘readiness’ according to three categories:
Survey of Mask readiness for Pilot line production

- Survey sent out end of September, responses lumped together into two categories:
  - Mask Infrastructure Suppliers – 5 organizations responded
    - Substrate/Blank, Mask, Metrology, Carrier
  - Mask Users – 7 organizations responded
    - 3 semiconductor companies
    - 3 semiconductor research consortia
    - 1 scanner company

- Responses used to color-code risk in ‘fishbone’ diagram of Mask Manufacture and Use.
  - Green/yellow/red color added if ≥ 25% of opinioned responses were in that category (responses in the no opinion category were ignored).
EUV Mask Infrastructure Readiness
2010 – 2012 Pilot Lines
Industry-wide Viewpoint

Color shown only if ≥ 25% respondents voted that way
EUV Mask Infrastructure Readiness
2010 – 2012 Pilot Lines
Users Viewpoint

Color shown only if ≥ 25% respondents voted that way

* Increased risk
! Lowered risk
Compared to all inputs

No work yet or late. WILL NOT BE READY
Projects or Tools underway. SHOULD BE READY
READY NOW
Users Perceived Critical Issues:

- LTEM Substrate:
  - Polish Defects
  - Defect Inspection
  - Defect Analysis

- LTEM Blank:
  - Deposition (defects)
  - ML Inspection
  - Defect Analysis
  - Defect Repair

- Pattern Inspection:
  - Pattern Defect Inspection
  - Full field Actinic Inspection

- Pattern Repair
  - FIB repair
  - Small field Actinic Inspection

- Exposure
  - Scanning (no pellicle, no pod)

- Fab Defects
  - In-fab Defect Inspection
  - In-fab Defect Clean
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  - Defect Analysis

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  - Deposition (defects)
  - ML Inspection
  - Defect Analysis
  - Defect Repair

- **Pattern Inspection:**
  - Pattern Defect Inspect
  - Full field Actinic Inspect

- **Pattern Repair**
  - FIB repair
  - Small field Actinic Inspect

- **Exposure**
  - Scanning (no protection)

- **Fab Defects**
  - In-fab Defect Inspect
  - In-fab Defect Clean
Discussion – Defects

1. Shift ebeam patterns to bury
2. Map pattern defects
3. Absorber defects repair

- Add Absorber, Resist
- Add Fiducials
- Select for layer use
- Map ML defects
- Map ML contacts
- Map ML gate
- Map ML defects
- Use rough coordinates from ML or LTEM inspect
- LTEM defects
- Add ML smoothing
- LTEM front Bevels behind
- Deposit ML/cap
- Rotate ML Blank if helps?

LTEM inspect ??
ML inspect ??
ML inspect ??
ML Defect repair ??

10 2 October 2008 IEUVI Mask TWG Meeting, Lake Tahoe, CA
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