EUV Mask Readiness:
Pilot Line 2010 - 2012

EUV Mask Readiness for Pilot Line

- It's Showtime for EUVL
  - We have about 2 to 3 years to enable EUVL Pilot Lines for at least two of our member companies.
  - If EUVL fails to work in these pilot lines then the future is bleak for EUVL.
- We need to concentrate on high risk items
  - Resources are limited
- IEUVI Task:
  - Identify current high-risk 'Will Not Be Ready' issues facing pilot-line readiness
    - Highlight those issues where new projects could help
    - Identify work-around options where high risk is unavoidable

Survey of Mask readiness for Pilot line production

Respondents asked to rate their perception of EUV Mask Infrastructure Readiness for Pilot Line Manufacturing: 2010-2012

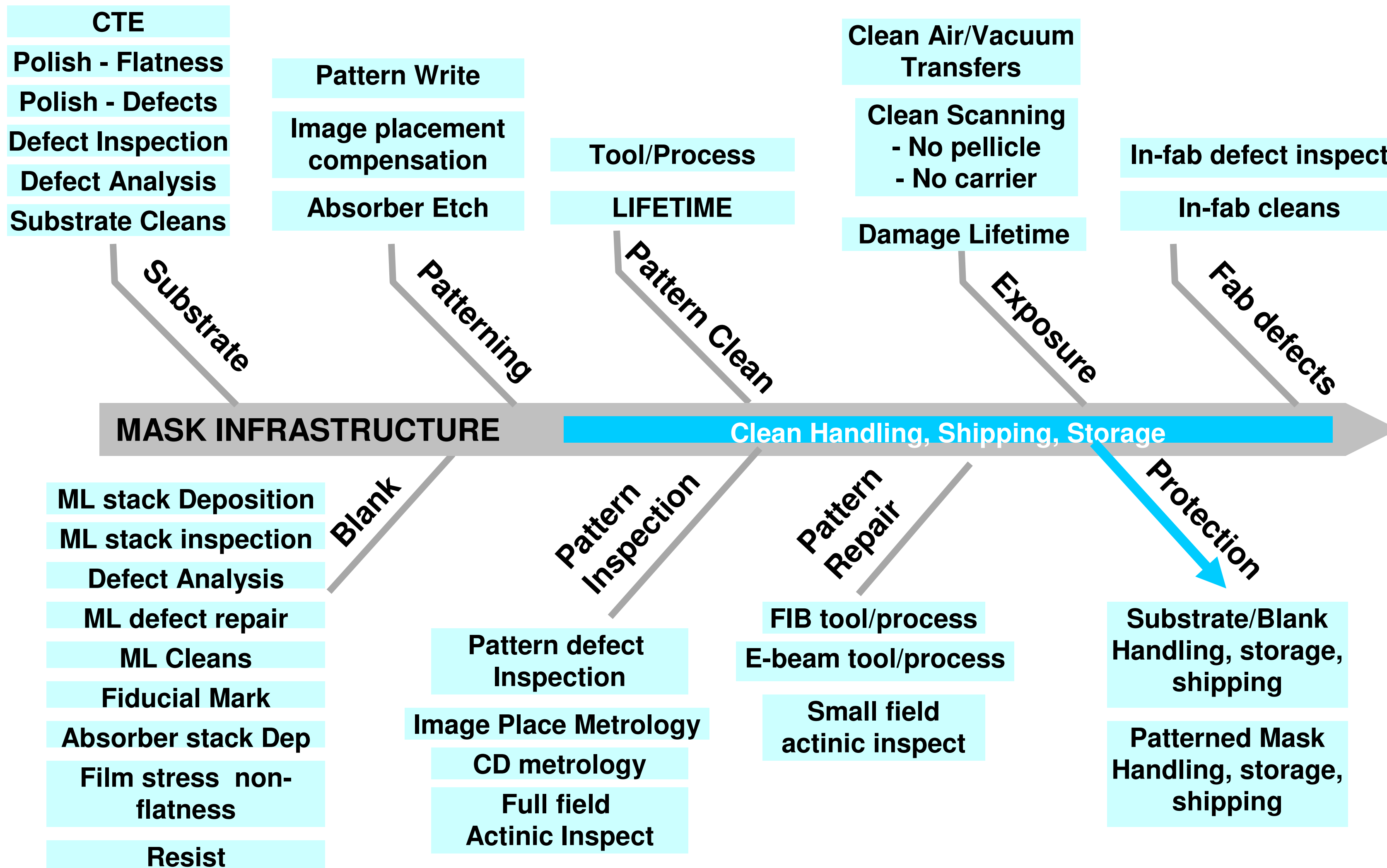
Key requirements from the ITRS Roadmap for EUVL Masks were included for use in judging readiness.

ITRS REQUIREMENTS	2010	2011	2012	2013
Mask Nominal Feature Size	120nm	107nm	95nm	85nm
(Nominal Feature Size at Wafer)	(30nm)	(27nm)	(24nm)	(21nm)
Mask 3σ CD uniformity MPU gates	2.7nm	2.4nm	2.1nm	1.9nm
Mask 3σ CD uniformity DRAM dense	5.2nm	4.6nm	4.1nm	3.7nm
Mask Image Placement, max error	5.4nm	4.8nm	4.3nm	3.8nm
LTEM substrate flatness peak/valley	51nm	46nm	41nm	36nm
LTEM substrate minimum defect size	35nm	33nm	31nm	30nm
Mask minimum defect size	40nm	36nm	32nm	29nm

Asked to classify 'readiness' according to three categories:

It is Ready Now	Projects or Tool Program Underway, Should be Ready	No Work Underway or Late, Will Not be Ready

EUV Mask Infrastructure Fishbone



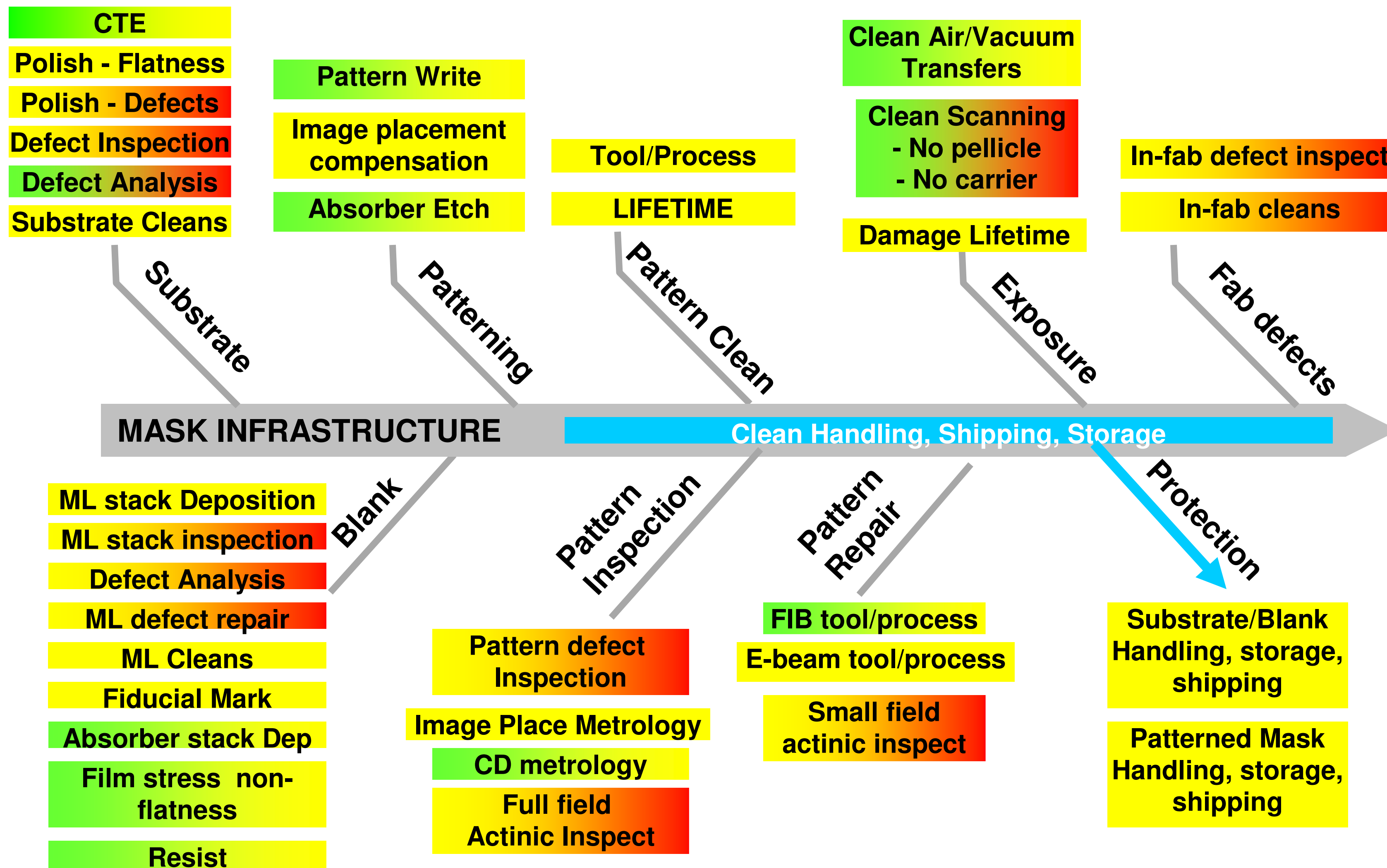
Survey of Mask readiness for Pilot line production

- Survey sent out end of September, responses lumped together into two categories:
  - Mask Infrastructure Suppliers – 5 organizations responded
    - Substrate/Blank, Mask, Metrology, Carrier
  - Mask Users – 7 organizations responded
    - 3 semiconductor companies
    - 3 semiconductor research consortia
    - 1 scanner company
- Responses used to color-code risk in 'fishbone' diagram of Mask Manufacture and Use.
  - Green/yellow/red color added if ≥ 25% of opinioned responses were in that category (responses in the no opinion category were ignored).

EUV Mask Infrastructure Readiness
2010 – 2012 Pilot Lines
Industry-wide Viewpoint

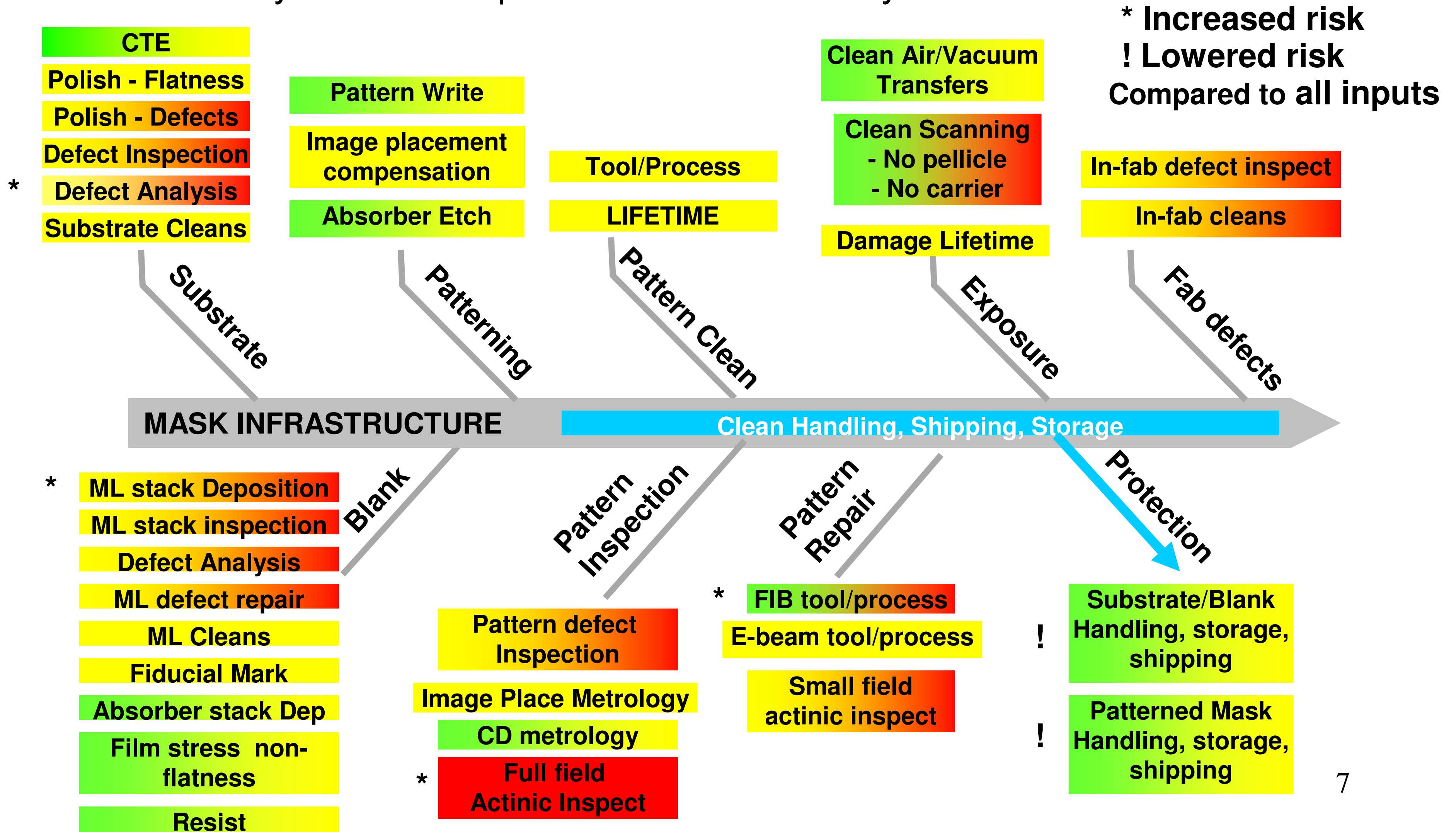
- Red: No work yet or late. WILL NOT BE READY
- Yellow: Projects or Tools underway. SHOULD BE READY
- Green: READY NOW

Color shown only if ≥ 25% respondents voted that way



EUV Mask Infrastructure Readiness
2010 – 2012 Pilot Lines
Users Viewpoint

Color shown only if ≥ 25% respondents voted that way



Users Perceived Critical Issues:

- LTEM Substrate:
  - Polish Defects
  - Defect Inspection
  - Defect Analysis
- LTEM Blank:
  - Deposition (defects)
  - ML Inspection
  - Defect Analysis
  - Defect Repair
- Pattern Inspection:
  - Pattern Defect Inspection
  - Full field Actinic Inspection
- Pattern Repair
  - FIB repair
  - Small field Actinic Inspection
- Exposure
  - Scanning (no pellicle, no pod)
- Fab Defects
  - In-fab Defect Inspection
  - In-fab Defect Clean

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  - Pattern Defect Inspect
  - Full field Actinic Inspect
- Pattern Repair
  - FIB repair
  - Small field Actinic Inspect
- Exposure
  - Scanning (no protection)
- Fab Defects
  - In-fab Defect Inspect
  - In-fab Defect Clean

Discussion – Defects

LTEM front
Bevels behind

Deposit
ML/cap
ML
smoothing

Rotate ML
Blank if
helps ?

Add
Fiducials

Select for
layer use

Add
Absorber,
Resist

Map ML
defects

metal

1. Shift
ebeam
patterns
to bury

Map ML
defects

contacts

2. Map
pattern
defects

Map ML
defects

gate

3.
Absorber
defects
repair

LTEM
inspect
??

ML
inspect
??

Use rough
coordinates
from ML or
LTEM inspect

ML Defect
repair??

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