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IEUVI Mask Technical Working Group

Proposed changes P37/P38/P40 SEMI standards

Thursday, Feb 28, 2008

Introduction

- All of the recommendations are driven by the need to meet overlay, particles and manufacturability requirements for reticles
- General Recommendations for P37 and P38
  - Consolidate into one standard: EUV Mask Blank
  - Update standards towards 16nm node
- General Recommendations for P40
  - Change the requirements so that empirical compliance to the standard can be met independent of the mounting method

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SEMI P37

Specific Proposals

P-37 Review Summary

- Separate both Tilt and Bow from flatness requirements
  - Redefine flatness to allow bow and tilt removal
  - Add table for allowable Bow
- Table 4 – Flatness Error in Flatness Quality Area
  - Update to include 16 nm node
  - Review need to have Low Order Thickness Variation in this table
  - Review local slope of front surface
  - Add local slope for back side
- Review the Defect requirements
  - Backside may not be tight enough
  - Front side will need classes of defects
- Modify/review the CTE temperature measurement conditions
- Review chamfer (Asahi Glass Co. Proposal)

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Definition of flatness should have the Bow removed – otherwise it will be impossible to make reticles

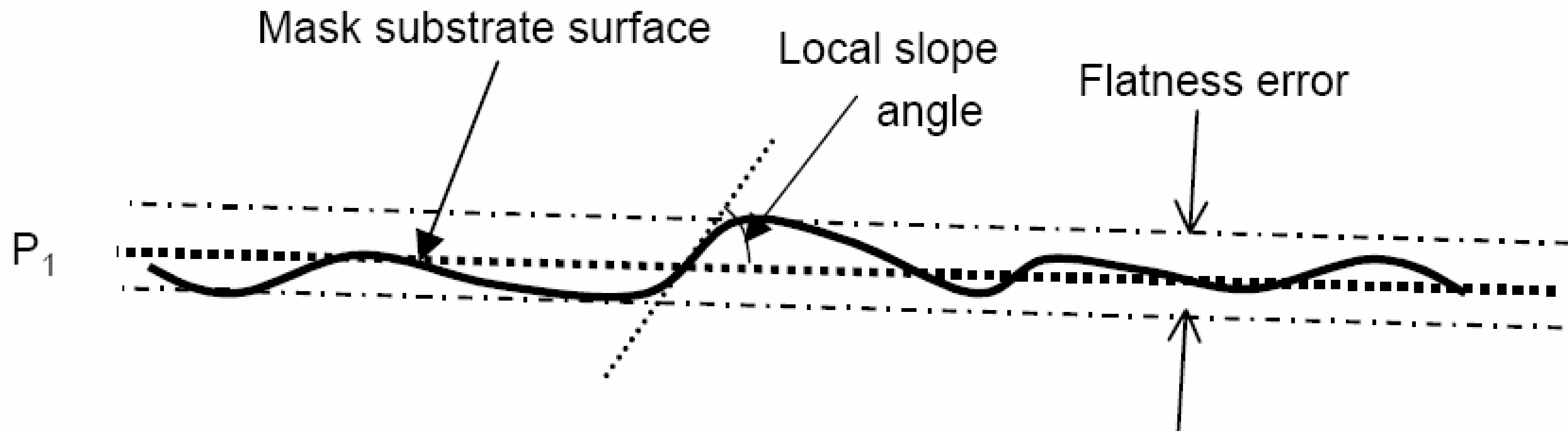

Figure 4
Definition of Flatness Error and Local Slope Angle
P1 is the plane that minimizes maximum deviation of the surface.

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P1 is the plane after bow removal that minimizes the maximum deviation of the surface

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Flatness requirements need to be extended to beyond the 32nm node requirements

Review LOTV

Table 4 Flatness, Wedge and Surface Roughness

FLATNESS ERROR IN FLATNESS QUALITY AREA

Class	*Frontside Flatness, within Flatness Quality Area*	*Backside Flatness, within Flatness Quality Area*	*Low Order Thickness Variation (LOTV), within Flatness Quality Area (See Note 2.)* $\lambda_{spatial}$ > *(edge length)*	*Units*
A	100 peak-to-valley	100 peak-to-valley	100	nm
B	75 peak-to-valley	75 peak-to-valley	75	nm
C	50 peak-to-valley	50 peak-to-valley	50	nm
D	30 peak-to-valley	30 peak-to-valley	30	nm

NOTE 1: $\lambda_{spatial}$ is the spatial period of the flatness error.
NOTE 2: Evaluated after removing wedge angle.

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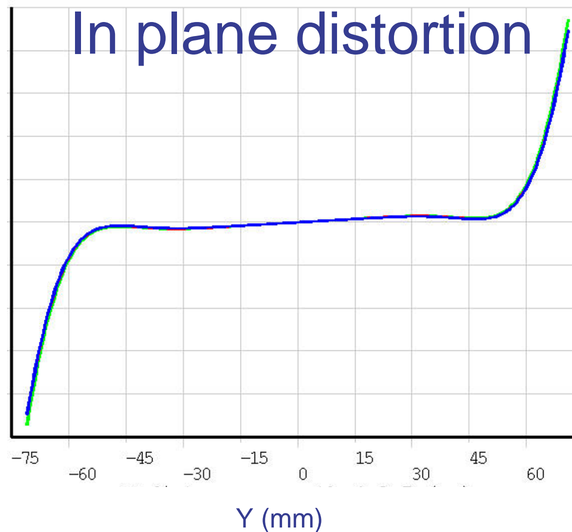
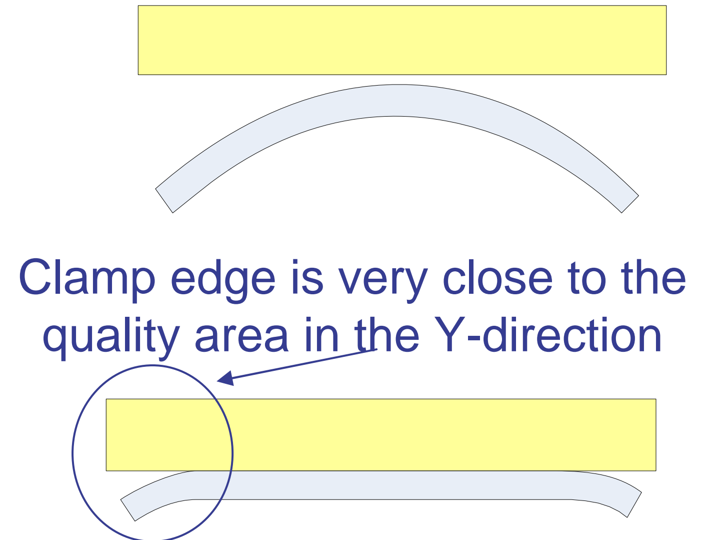
When clamped, reticle bow adds primarily in plane distortion (IPD)





- Reticle bow does not lead to a fully linear distortion due to edge effects of the clamp
- Even withclamp optimization, bow less than 1µm is needed to meet the targeted overlay

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ASML proposal to extend the flatness table

Table 4

Flatness Error (nm) in Flatness Quality Area

Review LOTV

Class	Frontside Flatness (P-V)	Backside Flatness (P-V)	Low Order Thickness Variation λ > edge length	Bow*
~~A~~	~~100~~	~~100~~	~~100~~	
~~B~~	~~75~~	~~75~~	~~75~~	
C	50	50	50	
D	30	30	30	600
E	23	23		400
F	16	16		300

* The Bow must be the final bow after all patterning (A reason for combining P-37 and P38)

- Recommendation: Remove classes that are in conflict with planned implementation of EUV and would not supported the targeted overlay

Bow = $\text{Range}[a_{20}x^2 + a_{02}y^2]$ x,y in quality area

Where a_{20} and a_{02} are defined $Z = \sum a_{ij} X^i Y^j$

Certain processes and procedures can cloud this (non) requirement

Table 5 Substrate Defect Limits per Plate

FRONTSIDE SURFACE DEFECTS IN THE DEFECT QUALITY AREA

Frontside	*Residue*	*Total Scratch and Sleek Defects > 1 nm in depth (See Note 1.)*	*Total Localized Light Scatterers > 50 nm PSL equivalent size (per cm^2) (See Note 2.)*	*Total Localized Light Scatterers < 50 nm PSL equivalent size (per cm^2) (See Note 2.)*
NZTE	None	0	0	To be agreed upon between user and supplier

NOTE 1: The maximum size for scratches and sleeks will be agreed upon between user and supplier.
NOTE 2: Localized light scatterers are any isolated features, such as particles or pits, on or in the substrate surface, resulting in increased light scattering intensity relative to that of the surrounding substrate surface. PSL equivalent size means the detected defect appears to be the same size as a polystyrene latex sphere examined under the same inspection conditions.

Entire topic needs to be reviewed

Does the (non) specification belong in the standard since there are compensation techniques (eg use of fiducials and/or smoothing)?

If in the standards for guidance, should establish classes like ML.

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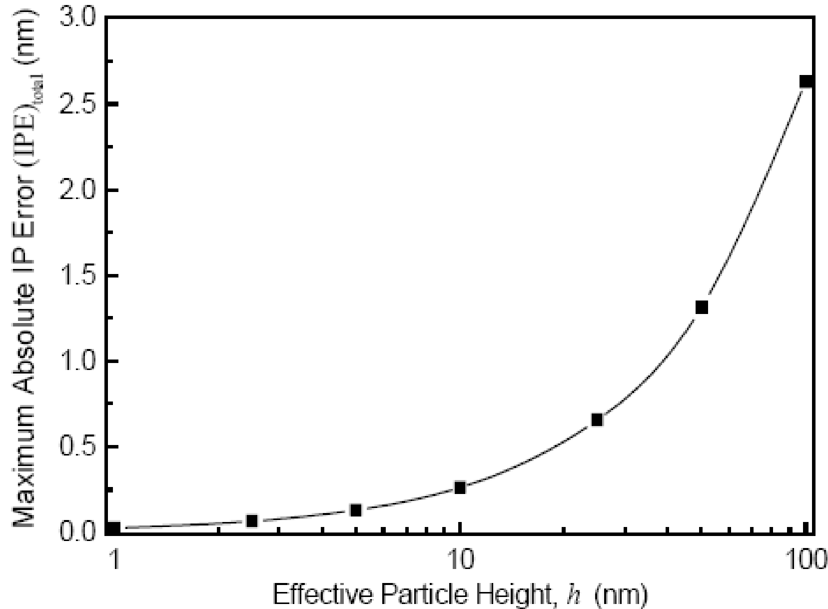
Backside defects in the flatness quality area may be too large

BACKSIDE DEFECTS IN FLATNESS QUALITY AREA

Localized Light Scatterer Size (PSL equivalent) (See Note 2.)	*Total*	*Total Number of Backside Scratches (See Note 1.)*
> 1.0 µm	0	0
≤ 1.0 µm	no limit	

NOTE 1: The maximum size for scratches and slecks will be agreed upon between user and supplier.

NOTE 2: Localized light scatterers are any isolated features, such as particles or pits, on or in the substrate surface, resulting in increased light scattering intensity relative to that of the surrounding substrate surface. PSL equivalent size means the detected defect appears to be the same size as a polystyrene latex sphere examined under the same inspection conditions.



Effective height of reticle backside particle may need to be below 40nm

Once coated, particles might not be deformable

Vasu Ramaswamy, 25th Annual BACUS Symposium on Photomask Technology, edited by J. Tracy Weed, Patrick M. Martin, Proc. of SPIE Vol. 5992, 59923T, (2005)

ASML Proposal for Backside defects in the flatness quality area

Table 5

Backside defects in the defect quality area

Localized Light Scatterer Size (PSL equivalent) (See Note 2.)	Total	Total Number of Backside Scratches (See Note1.)
> 0.1 µm	0	0
≤ 0.1 µm	No limit	

- Here we've assumed that the force of the clamp will crush any type of coated particle below 100nm

CTE spec does not match the operating temperature range for high-volume tools

Property	*Symbol*	*Characteristic*
Temperature range for CTE requirement		19 to 25°C
Coefficient of Thermal Expansion	CTE (ppb/°C)	Class A: mean: 0 ± 5 ppb/°C 6 ppb/°C total spatial variation Class B: mean: 0 ± 10 ppb/°C 10 ppb/°C total spatial variation Class C: mean: 0 ± 20 ppb/°C 10 ppb/°C total spatial variation Class D: mean: 0 ± 30 ppb/°C 10 ppb/°C total spatial variation

- For High T-put tools the reticle operating temperature will be substantially higher than 25°
  - Current estimates with 67% reticle reflection, heat conductivity of 1.5 W/m·K, reticle thickness 6.35 mm, show operating temperatures of 50…80°C
- At operating temperatures 50…80°C, CTE of current LTEM materials will largely exceed allowed values
- Thermal expansion specification needs to be reviewed

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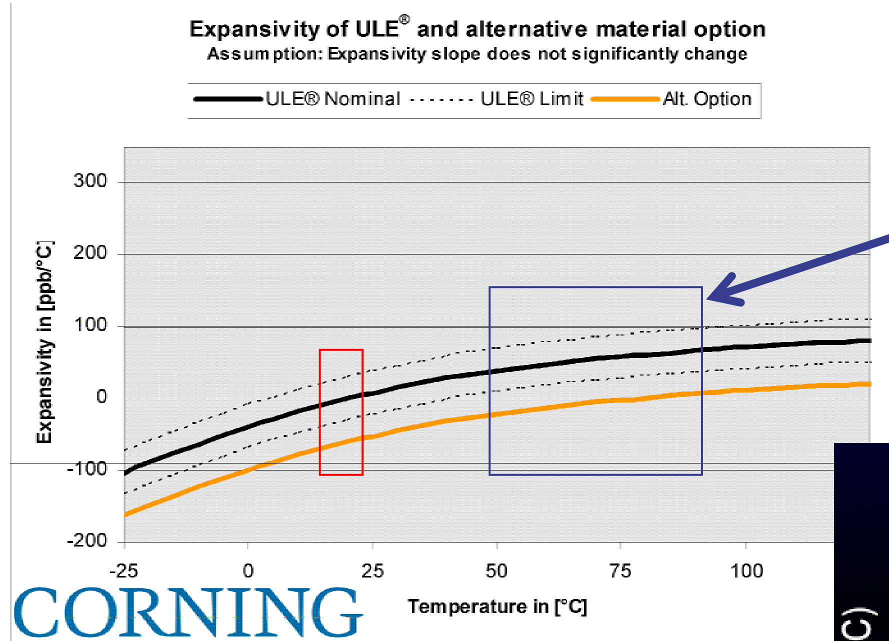
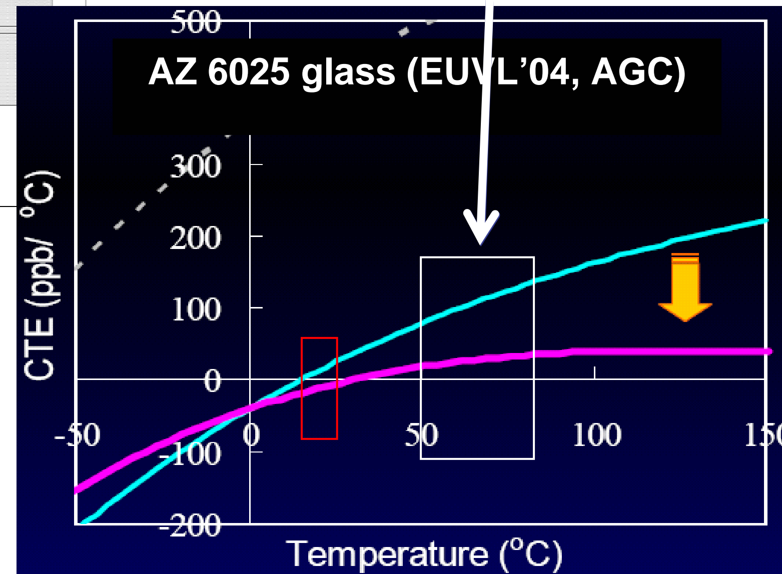
LTEM materials can be tailored for a specific cross over temperature



Expected reticle operating temperature range for High T-put HVM



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Task force should review the CTE issue and potential solutions

- Industry must understand the situation
  - Reticle use and impact on temp
    - Power
    - Effective reflectivity
    - Heat conductivity
- Possible solutions for compensating the expected operating conditions for high throughput
  - Cross over temperature modifications
  - Higher thermal conductivity materials
  - Thinner reticles

Chamfer may need to be opened up to make reticle less prone to edge chipping

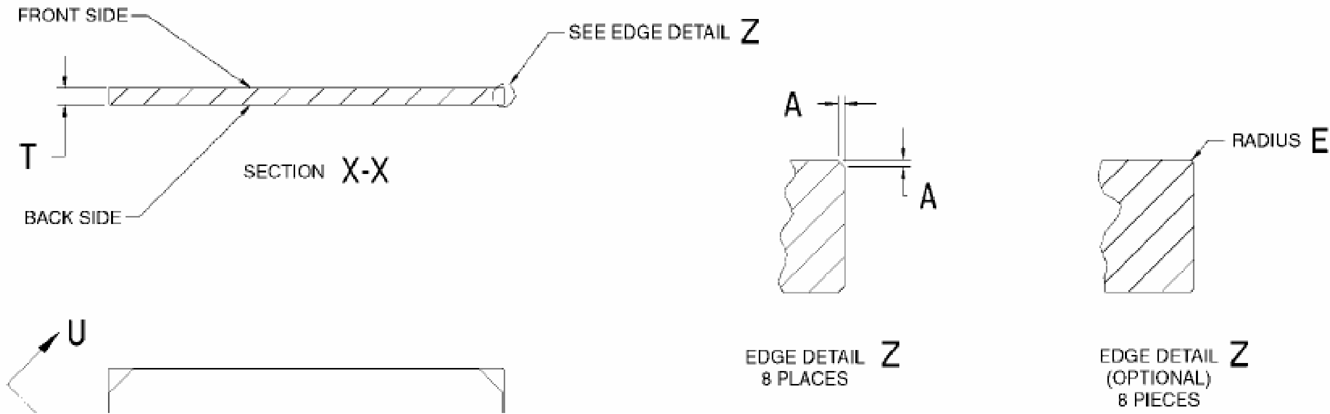

Table 2 Specifications for Chamfered and Rounded Edge Dimensions

T	*A*	*A*	*C*	*C*	*D*	*D*	*E*	*E*	
Nominal	*Min.*	*Max.*	*Min.*	*Max.*	*Min.*	*Max.*	*Min.*	*Max.*	*Units*
6.35	0.20	0.30	0.30	0.70	0.50	1.00	0.25	0.30	mm

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SEMI P-38

Specific Proposals

P-38 review summary

- Much of the document leaves most of the parameters up to the user and the supplier. If there are no agreed standards then these parameters should be put into an appendix.
  - This would be similar to substrate physical properties in P37
- Table 4 – Median Wavelength and BW of EUV Reflectivity of ML stack
  - Have user define the centroid wavelength wanted:
    - Peak
    - Median
- Table 13 – Defect Requirements for Multilayer stack
  - Update to include 16nm node
- Table 14 – Defect Requirements for Absorber stack
  - Update to include 16nm node

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User should define the wavelength spectrum centroid

Table 4 Median Wavelength And Bandwidth Of EUV Reflectivity Of Multilayer Stack

Mean FWHM of reflectivity versus wavelength	> 0.50 nm
Mean median reflected wavelength	Agreed upon between user and supplier

Note 1: Mean is determined from measurements made at different spatial locations on the mask blank surface. Sample size and measurement locations for determining mean are to be agreed upon between user and supplier.

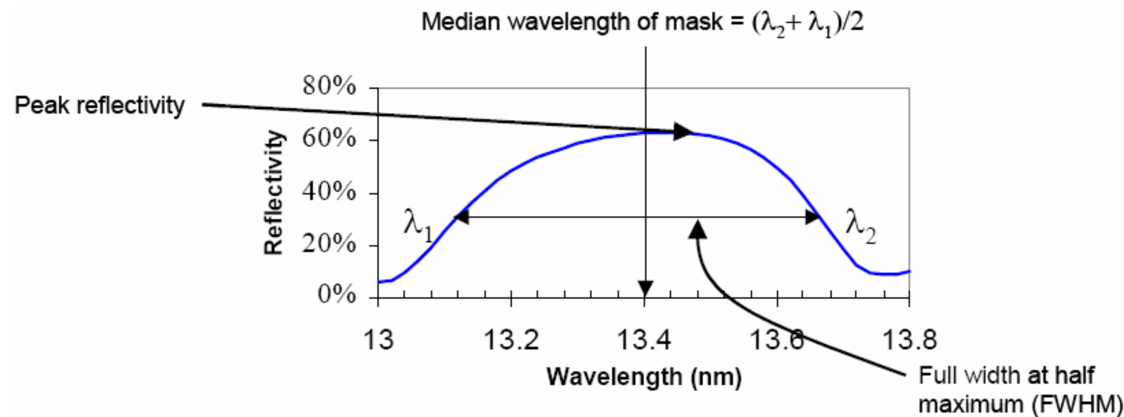

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Table 4 Median wavelength and BW of EUV Reflectivity of multilayer stack

Mean FWHM of reflectivity Vs wavelength	> 0.50 nm
Center wavelength definition	Agreed upon between user and supplier (Either median or peak)
Mean reflected center wavelength	Agreed upon between user and supplier

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Defect requirements for multilayer stack needs update

Table 13 Defect Requirements for Multilayer Stack

Class	*PSL equivalent size range (nm) (See Note 1.)*	*Maximum defect count*
A	> 25	0
B	> 30	0
C	> 40	0
D (Test)	> 60	Agreed upon between user and supplier

Note 1: PSL equivalent size means the detected defect appears to be the same size as a polystyrene latex sphere examined under the same inspection conditions. Defect count for defects with size smaller than that shown is not specified.

Proposal: Reverse the order 60 – 25 (corresponds to A – D) and add E, F and G

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ASML Proposal for ML stack defect requirements

Table 13 Defect Requirements for multilayer stack

Class	PSL equivalent size range (nm) (See note 1)	Maximum defect count
~~A~~	~~>90~~	~~Agreed upon between user and supplier~~
~~B~~	~~>60~~	~~Agreed upon between user and supplier~~
C	>40	0
D	>30	0
E	>25	0
F	>18	0
G	>13	0

- Remove classes that are in conflict with planned implementation of EUV at the 32nm node and below
- Reverse the order to ease Standard maintenance

Defect requirements for the absorber stack needs update

Table 14 Defect Requirements for Absorber Stack

Class	*Defect size range (nm) (See Note 1.)*	*Maximum count*	*Defect size range (nm) (See Note 1)*	*Maximum count*
A1	15–180	0	> 180	0
A2	15–180	10	> 180	0
B1	25–265	0	> 265	0
B2	25–265	10	> 265	0
C1	35–360	0	> 360	0
C2	35–360	10	> 360	0
D1	50–520	0	> 520	0
D2	50–520	10	> 520	0
E (Test)	< 1000	1500	> 1000	0

Note 1: PSL equivalent size means the detected defect appears to be the same size as a polystyrene latex sphere examined under the same inspection conditions. Defect count for defects with size smaller than that shown is not specified.

Proposal: Reverse the order and add more rows.

It is unclear what the value is of having A1 and A2 by changing the max counts.

ASML Proposal for absorber stack defect requirements

Table 14 Defect Requirements for absorber stack

Class	PSL equivalent size range (nm) (See note 1)	Maximum count (n = 0 or 10)	Defect size range (nm) (See note 1)	Maximum count
~~A_{1500}~~	~~<1000~~	~~1500~~	~~> 1000~~	~~0~~
~~B_n~~	~~50 – 520~~	~~n~~	~~> 520~~	~~0~~
C_n	35 – 360	n	> 360	0
D_n	25 – 265	n	> 265	0
E_n	15 – 180	n	> 180	0

- Remove classes that are in conflict with planned implementation of EUV at the 32nm node and below
- Reverse the order to ease Standard maintenance

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SEMI-P40

Background

ITRS roadmap and SEMI Standards values for reticles and clamps are necessary to meet the 5.7nm 32nm node overlay target

Representative Budget (nm)	ITRS + P-40	ITRS + P-40 & No Dedication
Tool	**3.2**	**4.5**
Process	**1.5**	**1.5**
Exposure tool reticle clamp unflatness	**0.0**	**1.0**
IPD	0.0	0.8
OPD	0.0	0.6
Reticle clamped in exposure tool	**1.4**	**1.6**
Reticle writing	0.9	0.9
Reticle flatness	0.9	1.2
OPD	0.8	0.8
IPD	0.2	0.8
Bow	0.4	0.4
CTE non-uniformity	0.6	0.6
Total per layer	**3.8**	**5.1**
Layer to layer	**5.4**	**7.2**

Without tool dedication, the target overlay cannot be met

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SEMI P40 guides reticle clamping for all tools, but it should be revised to allow for flexibility in meeting requirements

- Although not explicitly stated, P40 assumes that all systems are using electrostatic clamps
- Of the “three rules” (chuck flatness, pressure, stiffness), not all are necessary, nor are they sufficient to assure that the mounted reticle distortion requirements are met
- For a kinematic clamp to meet the requirements, an agreed to metrology standard would need to be added to P-40 to show compliance with the requirements
  - The standard should be revised to show that empirically matching the requirements is allowed
  - A reference reticle blank and an interferometric test could be a possibility

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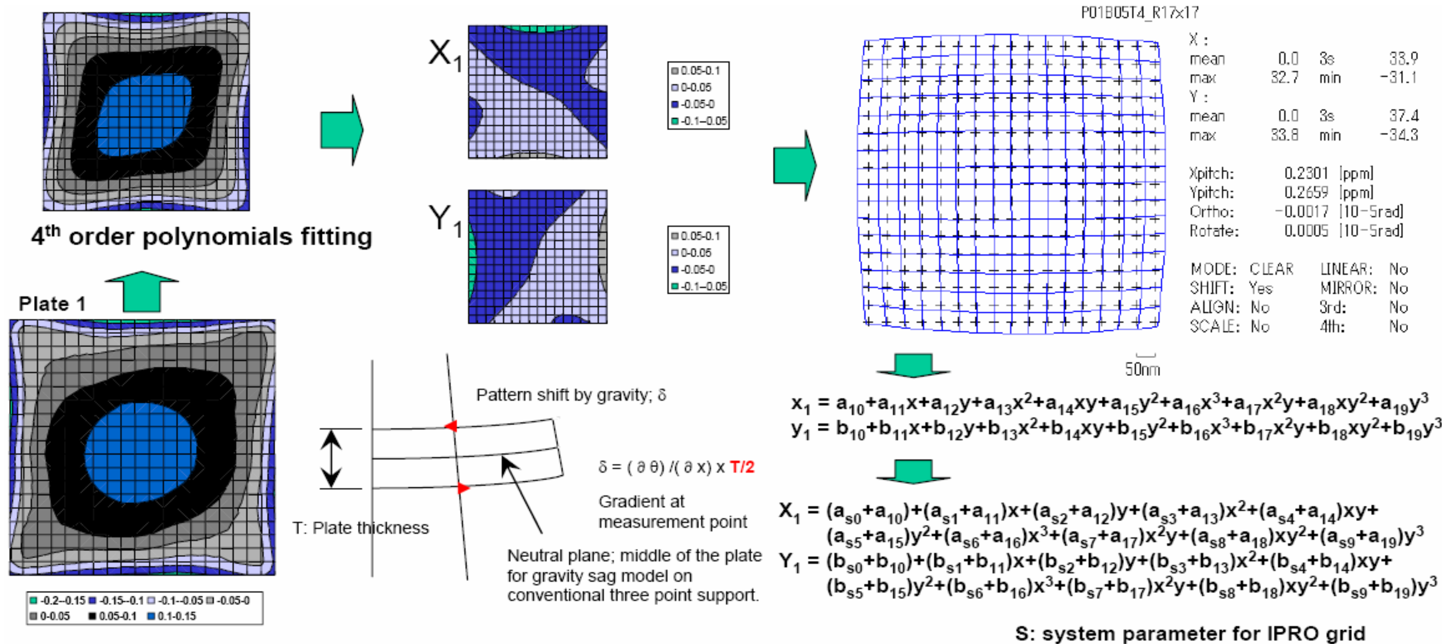
IPD error budget allocation will depend on the type of reticle clamping

- NuFlare has reported[1] an alternative to electrostatic clamping using kinematic clamping and software compensation plus a specially designed stiff chuck in the pattern placement metrology tool



$$x_1 = a_{10}+a_{11}x+a_{12}y+a_{13}x^2+a_{14}xy+a_{15}y^2+a_{16}x^3+a_{17}x^2y+a_{18}xy^2+a_{19}y^3$$
$$y_1 = b_{10}+b_{11}x+b_{12}y+b_{13}x^2+b_{14}xy+b_{15}y^2+b_{16}x^3+b_{17}x^2y+b_{18}xy^2+b_{19}y^3$$

$$X_1 = (a_{s0}+a_{10})+(a_{s1}+a_{11})x+(a_{s2}+a_{12})y+(a_{s3}+a_{13})x^2+(a_{s4}+a_{14})xy+(a_{s5}+a_{15})y^2+(a_{s6}+a_{16})x^3+(a_{s7}+a_{17})x^2y+(a_{s8}+a_{18})xy^2+(a_{s9}+a_{19})y^3$$
$$Y_1 = (b_{s0}+b_{10})+(b_{s1}+b_{11})x+(b_{s2}+b_{12})y+(b_{s3}+b_{13})x^2+(b_{s4}+b_{14})xy+(b_{s5}+b_{15})y^2+(b_{s6}+b_{16})x^3+(b_{s7}+b_{17})x^2y+(b_{s8}+b_{18})xy^2+(b_{s9}+b_{19})y^3$$

S: system parameter for IPRO grid

1. **Correction technique of EBM-6000 prepared for EUV mask writing, Yoshitake** et. al, **Photomask Technology 2007 SPIE Vol 6730-105**

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Proposed changes to P-40 that would allow more design flexibility in mounting EUV reticles

Parameter	Current P-40	Proposal
Mean clamping pressure (kPa)	15 ± 1.5	Delete
Max clamping pressure in contact area (kPa)	Not specified	≤ 3,000
P-V flatness-quality area (nm)	48	≤ 32
P-V flatness-sub aperture (nm) 75mm, etc	24, etc	Delete
Local slope error (μrad) (over 20mmx20mm)	Not Specified	≤ 1
Stiffness (Nm)	> 30,000	Review
Pin Pitch (mm)	< 10	Delete

Note that the suggested values are consistent with a 32nm overlay budget and that various quality levels would have to be added for subsequent nodes

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