

**Sapporo, November 2, 2007  
Sapporo Renaissance Hotel**

# **International EUV Initiative (IEUVI) Mask Technology Working Group (TWG) Report to IEUVI Board**

***Co chairs:***

***P. Seidel – SEMATECH,***

***K. Orvek – Intel / SEMATECH***

***O. Suga – SELETE***

***J-H Peters – AMTC***

***J. Ahn – Hayang Univ.***

**Phil Seidel\***

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# IEUVI Mask TWG Report

## Agenda:

- ◆ Mask TWG chair organization update
- ◆ Mask TWG representatives attending Nov 1<sup>st</sup> 2007 meeting
- ◆ Noteworthy EUV mask related progress by food chain area
  - Materials
  - Mask manufacturing and process tools
  - Mask printing performance / impacts
  - Mask handling, use maintenance, and standards
- ◆ Mask TWG Critical Issues Assessment
- ◆ Mask TWG Roadmap Update
- ◆ Key Mask TWG Messages For Board Membership
- ◆ 2008 Plans



# IEUVI Mask TWG Organization Update

## IEUVI Mask TWG Meeting Organizer:

Shinji Okazaki – ASET; returned to Hitachi w/ other responsibility.

No replacement

## IEUVI Mask Japan Co-Chair:

Iwao Nishiyama – ASET; transition to Selete, transferring IEUVI chair to:

Osamu Suga – SELETE; new Japan Co-Chair:

## IEUVI Mask U.S. Co-Chair / Lead Chair:

Phil Seidel – SEMATECH; transition to ISMI, transfer chair to:

Dr. Kevin Orvek – Intel / SEMATECH; new U.S. Co-chair and Lead:

## IEUVI Mask Korean Co-Chair:

Dr. Jinho Ahn – Hayang Univ: *no change*

## IEUVI Mask European Co-Chair:

Jan-Hendrik Peters - AMTC: *no change*



# IEUVI Mask TWG Members & Nov 1<sup>st</sup> Representation

**Alcatel**: Catherine Le Guet\*

**AMD**: Obert Wood\*, Bruno La Fontaine

**AMTC**: Jan-Hendrik Peters\* (EU Co-chair),

**Asahi Glass Company**: Shinya Kikugawa\*,  
Yoshitake Ikuta

**ASML**: John Zimmerman\*, Rogier  
Groeneveld

**Canon**: Yoshio Gomei\*, Phil Ware

**Corning**: Michael Mueller\*, Junichi  
Yokoyama

**CNSE – SUNY**: John Hartley\*

**DNP**: Naoya Hayashi\*, Tsukasa Abe

**EUVA**: Naomichi Abe, Masashi Ogawa

**IMEC**: Rik Jonckheere\*

**Intel**: Kevin Orvek (Chair, US Co-chair), Gil  
Vandentrop, Long He,

**Hayang Univ**: Jinho Ahn\* (KR co-chair)

**Hoya**: Tsutomu Shoki\*

**KLA – Tencor**: Matt Dilorenzo

**LBNL**: Eric Gullikson

**Lasertec**: Osamu Okabayashi, Hiroshi  
Asai

**Nikon NRCA**: Michael Sogard\*

**Nikon**: Suzuki Kazuaki, Tsuneyuki  
Hagiwara\*

**NuFlare Tech.**: Shusuke Yoshitake\*

**Qimonda**: Micheal Lering

**Samsung**: Gi Sung Yoon\*, Hakseung  
Han, Seung Sue Kim

**SELETE**: Osama Suga\* (JP co-chair),  
Hiroyuki Shigenura, Kazuya Ota,  
Takao Taguchi

**SEMATECH**: Phil Seidel (Chair, US Co-  
chair), Stefan Wurm\*

**Veeco**: Rajul Randive

**26 representatives attended**

\* Primary Rep.



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# Key EUV mask highlights (past 6 months incl. Symp)

## Materials

- Blank / Substrate Insp.
- Surface clean / prep
- ML dep.
- Capping

## Mask Mfg. & Pattern Tools

- Binary process dev
- Pattern Gen.
- Pattern Insp
- Def. Review
- PSM develop
- Pattern Def. Repair
- Surface clean / prep
- Pattern Placement

*Yielded Mask and Image*

- Iso / Dense Bias
- Flare comp on features
- Shadowing effect compen
- Defect Printability

## Printing Capability

- Carrier Development
- Mol. Contamination
- Fiducial mark Standard for blank def
- Substrate Stdrd (P37)
- Blank Stdrd (P38)
- Chucking Standard (P40)
- Handling / LP Standards (4466)

## Mask Handling Mask Use



# Key EUV mask highlights (past 6 mo & Symp)

## Materials

**Blank / Substrate Insp.**  
**LTEM**  
**Figure**  
**Finishing**  
**Surface clean / prep**  
**ML dep.**  
**Capping**

## SEMATECH MBDC IBSD / ML Dev (EUVL Symp)

- New champion 0.10 def/cm<sup>2</sup> @ 56nm PSL (Veeco) process without smoothing
- Median performance 7 def @ 67nm PSL = 4.5X improvement over a 3 mo. period.
- Top pareto limiter remains pits (75%)

## AGC LTEM developments (EUVL Symp)

- LTEM mean CTE improved 1 ppb/°C @ 22°C; ≤10 ppb/°C P-V; ± 3 ppb/°C spati.
- Excellent flatness improvements to 38nm FS, 48nm BS, and 61nm P-V LOTV
- Substrate and ML defect improved: (ML best at 0.05 def/cm<sup>2</sup> @ 83nm PSL)
- New absorber stack materials offered to increase inspection contrasts (A,B)

## Hoya Substrate and blank developments (EUVL Symp)

- Best ML total defects 0.20 def/cm<sup>2</sup> @ 54nm PSL
- Improved substrate flatness reach 84nm P-V FS / 56nm P-V BS (local polish)
- Low stress absorber stacks attaining ±20 MPa

## Corning ULE™ developments (SPIE 6517)

- Excellent ULE™ stria reductions improves MSFR P-V (6.6nm P-V MSFR)  
Overall ~ 3X reduction (meets P37)
- No impact to already low CTE performance (+/- 5 ppb/°C)



# Key EUV mask highlights (past 6 mo & Symp)

## Materials

Blank / Substrate Insp.  
LTEM Figure Finishing  
Surface clean / prep  
ML dep.  
Capping

## SEMATECH Material Benchmarking (EUVL Symp)

- 4X defect improvements over 18 months
- Excellent commercial supplier improvements multiple specs simultaneous (Def., reflectivity, wavelength and flatness)

## SEMATECH MBDC Cleans / Surface Prep Developments (Semicon West '07)

- Multiple technology dev. underway; demo'd 10nm defect removal capability and attained 0 substrate particles  $\geq$  30nm PSL
- Megasonic cleans improvements best chance for defect removal of > 10nm size
- Laser shock cleans effective at > 30nm sizes

## Substrate and Blank Defect Inspection Platforms (SPIE, EUVL Symp.)

- Lasertec M7360 perform. at MBDC improving 40nm for PSL QZ / 50nm PSL ML
- Siemens New optical defect inspection platform DX+ is available
- Actinic defect inspection, review tool at LBNL / SEMATECH (AIT) greatly improved
- Mirai actinic inspection platform developments underway to obtain 40nm FWHM / 1.5nm height sensitivity @ 2 hrs per blank TPT (2008 timing) (3% CD change on 40nm CD)

# Key EUV mask highlights (past 6 mo & Symp) #3

## Materials

Blank / Substrate Insp.  
Surface clean / prep  
ML dep.  
Capping

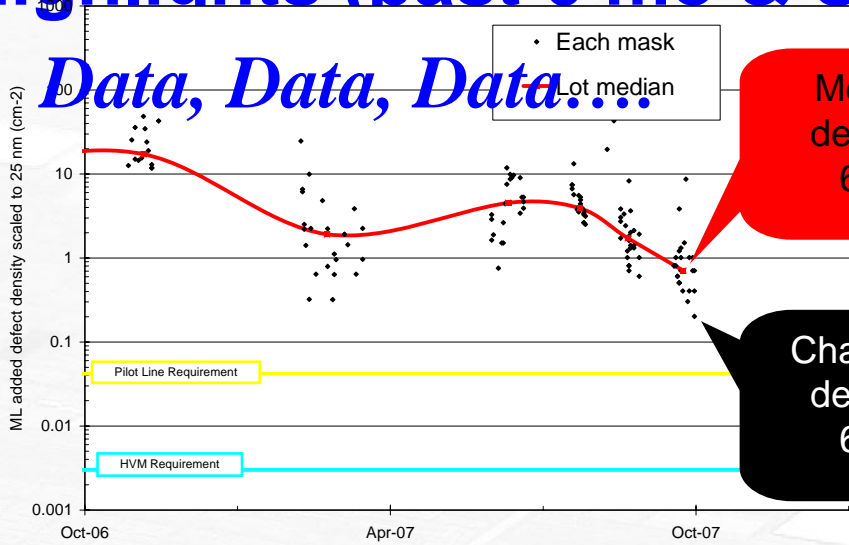
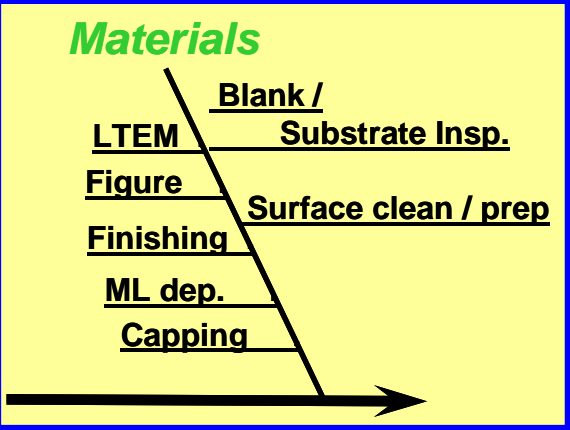
## imec Capping poster paper (EUVL Symp)

- Standard 11nm Si capped blanks , 3nm of Carbon no reflectivity change (w in +/- 0.5%)
- Ru 2-3 nm thick capped blank w/ 3nm of Carbon, 5% loss of reflectivity
- Can tweak the effect to make one more sensitive
- (absorption related effect, but the thickness film interference effect can be used to your benefit)

## S. Kim Samsung presentation on capping (EUVL Symp)

- Carbon deposition rate on Ru is lower than that of Si

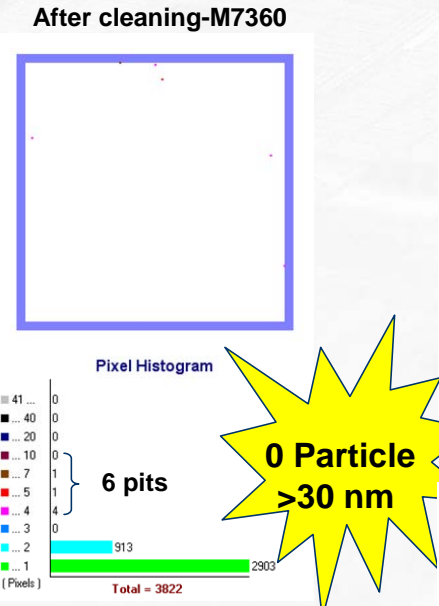
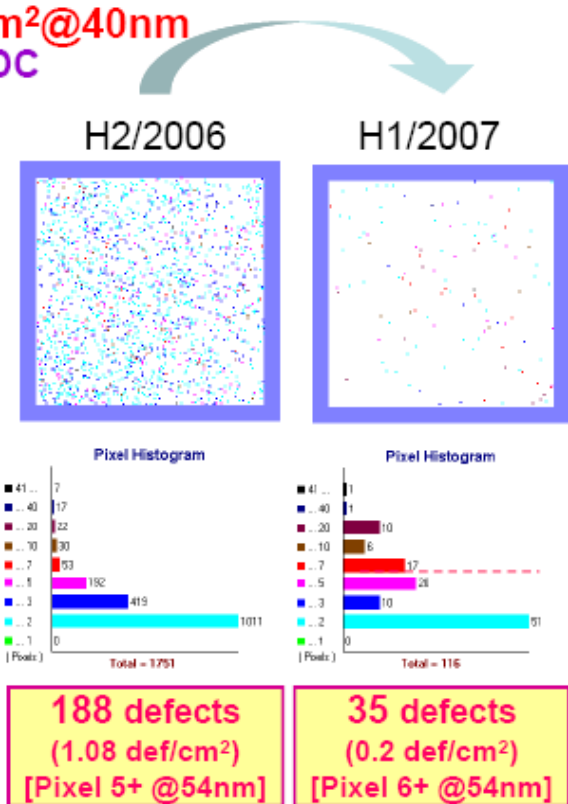
# Key EUV mask highlights (past 6 mo & Symp)



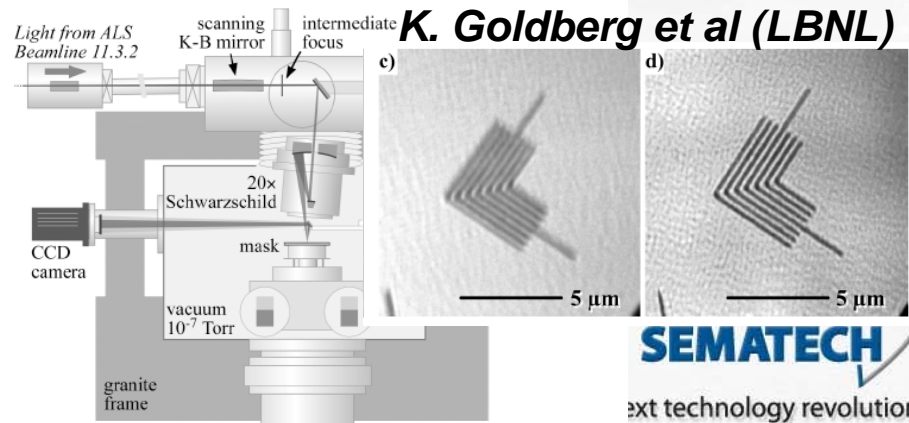
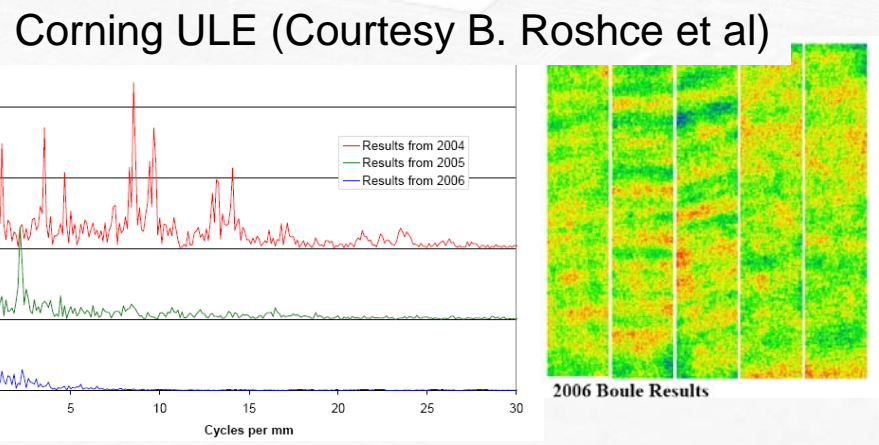
Median 7 defects at 67 nm

Champion 2 defects at 67 nm

Kearney, Jeon, et al  
SEMATECH MBDC / Veeco



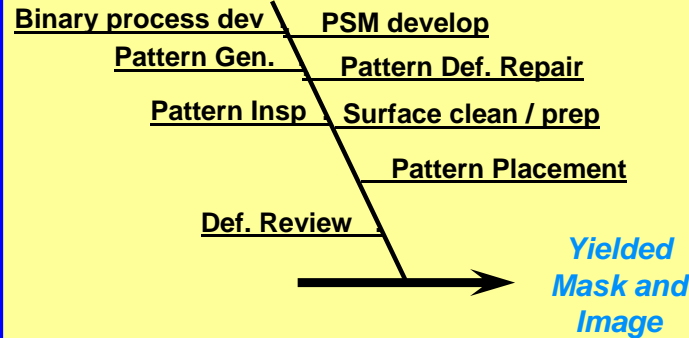
Data was confirmed by 4 times inspection on M7360  
**A. Rastegar et al (SEMATECH MBDC)**



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# Key EUV mask highlights (past 6 mo & Symp)

## Mask Mfg. & Pattern Tools



## NuFlare Technologies (SPIE PMJ)

- 45nm HP Pattern Generator system EBM-6000 showing write time decrease vs. EBM-5000
- 25% faster write 150 G shot, 10  $\mu\text{C}/\text{cm}^2$ , 2 pass write. A total of 12 hr write time for EBM-6000

## Carl Zeiss / SEMATECH 45nm / 32nm PP JDA

- Mask pattern placement inspection system for  $\leq 45\text{nm}$  (45nm and 32nm HP)

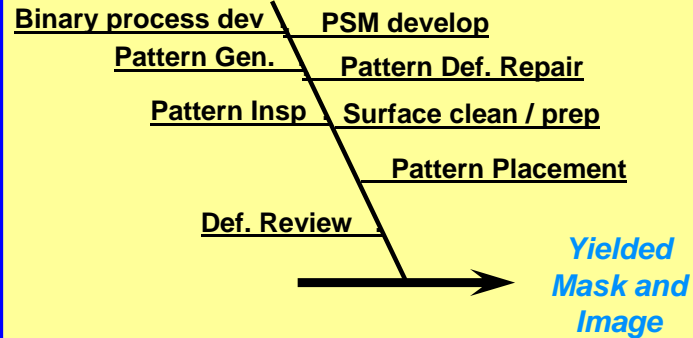
## Significant Commercial EUV Mask Developments by multiple companies

- Intel Mask House producing both small field and large field masks for internal and partnership activities including ASML ADT. (PMJ 2007 SPIE 6607)
  - Internal TaN absorber over Ru cap
  - Mask pattern resolution of 15nm (1X) CD DLS control 5.7nm; 7.4nm Iso.
  - Extensive work on blank / mask induced bow and clamping requirements
- Intel work on mask surface cleaning (Liang et al EUVL Symp.) showing that wet cleans with extension on SPM and SC1 and new capability DIO3 & DIH2
- DNP produce EUV F.F. masks for customers and partners Collaboration work with Intel (BACUS '07 6730)
  - Pattern profile demonstrated down to 150nm at mask
  - Iso. CD control 4.1nm (3s) and DLS CD control 5.2nm (3s)
  - Extensive programmed defect inspection testing shows DUV compatible for EUV



# Key EUV mask highlights (past 6 mo & Symp)

## Mask Mfg. & Pattern Tools



## Commercial EUV Mask Developments

- Samsung Mask House producing EUV full field masks for EUV developments and assorted tests masks (i.e. defect printability AIT at LBNL)
- AMTC producing full field masks for ADT set up masks & consortia (e.g. imec)

## Samsung patterned defect repair (EUVL Symp.)

- Samsung studied 15keV FIB, Nano Machining, and 30keV e-beam repair
- Ru and Si capping layer impact assessments show e-beam works better on Si and Ru cap compared to using FIB
- E-beam repair using Ru cap works better than FIB (scan damage)
- FIB repair on Ru cap shows strong scan damage at > 6 scans
- Nano Machining could be good approach L/S pattern, need improved accuracy
- e-beam repair shows no scan damage for either Si or Ru and could be best approach improved recipe required to reduce undercutting

## SELETE patterned defect repair (EUVL Symp.)

- SELETE investigating low accelerated voltage FIB combined with SEM and nano tweezer technology for defect repairs

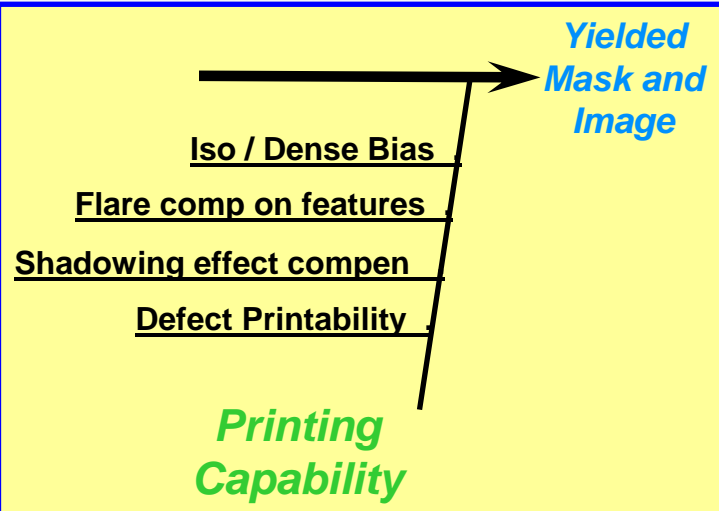
## SELETE and NuFlare 199nm Pattern Defect inspection (EUVL Symp)

- 50nm pixel capability tool; ~4X image contrast improvements through A.R. of patterned absorber thickness





# Key EUV mask highlights (past 6 mo & Symp)



## imec Defect Printability (EUVL Symp)

- Multiple defect cases simulated through modeling (Aerial image)
- Reinforces that 2.2nm – 2.3nm surface bump will cause a printed phase defect
- Carbon conformal contamination beginning at 2nm thickness will print
- Particle printability depends on the material composition

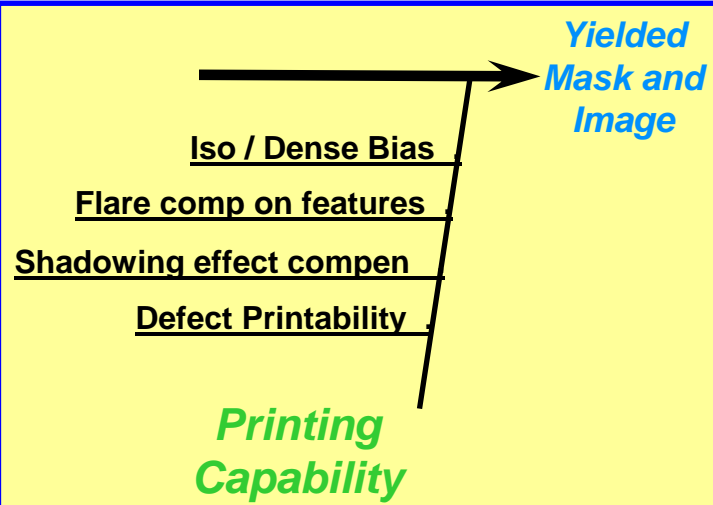
## Intel work on ML Phase Defect printability and growths (EUVL Symp)

- Modeling reinforces difference in surface defect structure in ML dep process.
- Aerial image defect printability study tends to under predict defect printability that could be caused by proximity effects, resist effects, and ML defect shapes
- 2.5nm x 50nm defect between lines appears to be most critical
- Near normal IBDS on defects causes 2.5nm height for < 30nm substrate defect
- Off normal IBSD causes extreme decorations (up to 25nm bump height)
- Smoothing highly desirable and defect covering with absorber should be developed further

## imec show new mask shadowing effects Poster Paper (EUVL Sym)

- Simulated predication of the shadowing effect on 50nm lines was confirmed experimentally

# Key EUV mask highlights (past 6 mo & Symp)



## AMTC report (EUVL Symp)

- AMTC fabricated a reticle for AMD that had shadow effects and flare compensation done by Mentor Graphics
- ASML printed complete chip on ADT

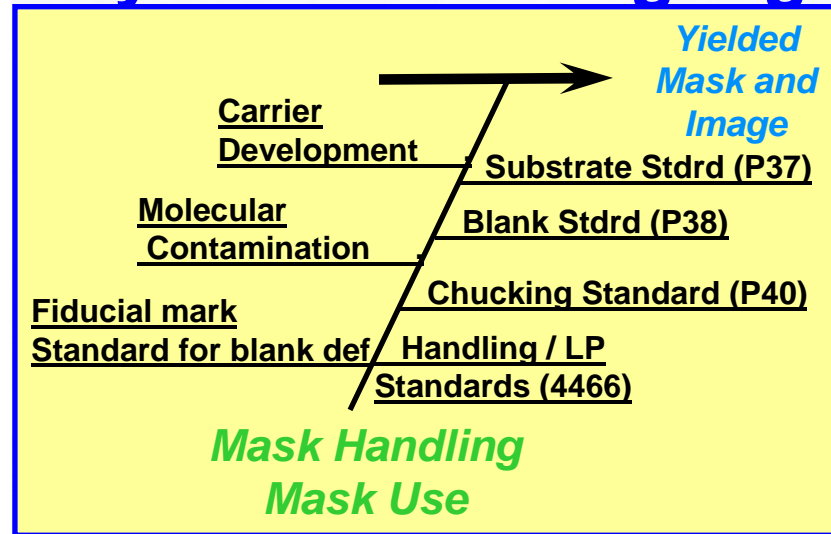
## NuFlare poster (EUVL Symp)

- Convincing data and approach on pattern correction to compensate for chucking issues in EUV. Exposure tool suppliers recognizing that we Do Not need Echucks on all tools.

## imec Flare correction Oral (EUVL Symp)

- Rule based correction is very effective for Flare compensation.

# Key EUV mask highlights (past 6 mo & Symp)



## Entegris / SEMATECH Carrier Dev. (EUVL)

- Entegris sPOD combined with shuffler has shown < 0.5 particle adders per 100 mechanical handling cycles (@ 50nm PSL).
- Defect adders < 0.3 per RT shipment
- Defect inspection sensitivity limitation 50nm for reticle handling
- New shuffler tool at MBDC

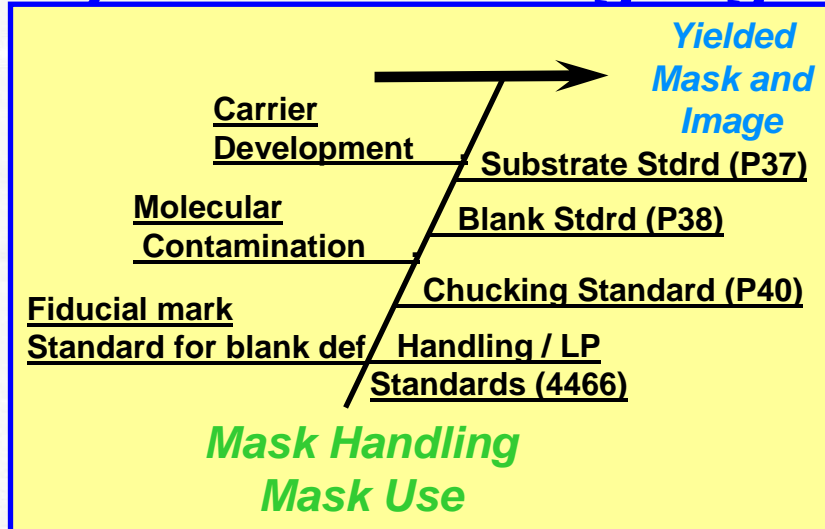
## SELETE support & testing of joint Canon / Nikon Dual Pod (EUVL Symp)

- SELETE using new testing system for carrier testing from Rorze Corp.
- Data shows improved Dual Pod performance with particle adder reduction of 53X improvement in Air Load Lock, 6.7X improvement in Air, and 3.3X improvement in Pod cycles.

## Kick-off meeting for SEMI Standard for fiducial marking for blanks to support defect mitigation strategies (P.Y. Yan – Intel / P. Seidel) Feb '07

- High interest but extensive coordination between inspection / metrology tools vs. pattern generator community needed
- Concern defect inspection tools today have limited accuracy for defect location to allow discrete defect covering using small pattern sizes (10X–100X improv.)
- Need to re-establish interest and momentum in '08

# Key EUV mask highlights (past 6 mo & Symp)



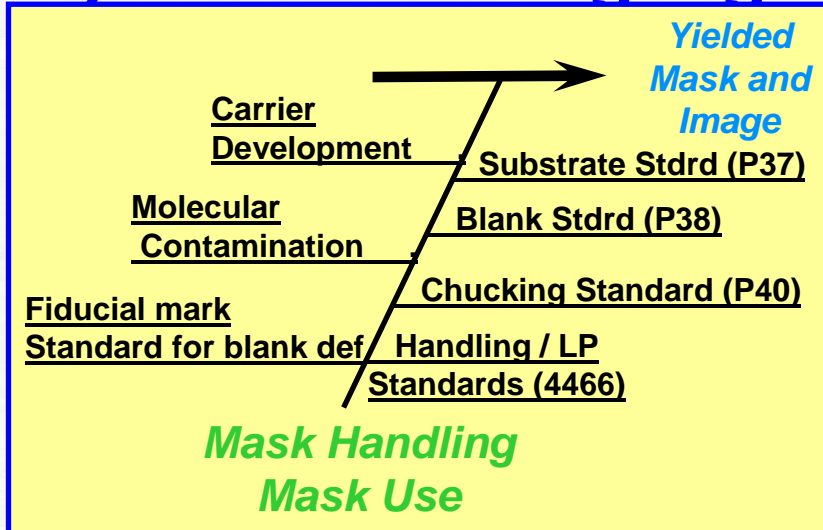
## EUV Carrier & Load Port Standard SEMI Ballot 4466 (EUVL)

- Successful Blue ballot in June '07 with comments / negative votes being resolved
- IP material classification completed (35) cases and 2 patents need IP disposition
- Yellow voting ballot (international ballot) targeted for Jan 2008 release

## ASML proposal to improve substrate / mask non flatness and chucking P40 & P37 modifications (EUVL Symp)

- ASML completed rigorous mask non flatness / OL error tolerances with current capability planned for EUV mask surface level changes (wedge, curvature, roll)
- ASML supports that PG chucking and induced bow can be minimized by PG SW writing compensation (NuFlare, Hoya, IMS Chips activity).
- However P40 needs to be rewritten to force a “global” flatness < 32nm P-V requirement and mask backside local slope error < 1 urad/ over 20mmx20mm
- Previous P40 terms of Mean clamping pressure, sub-aperture non flatness of < 75nm P-V, and chuck pin pitch spacing to all be DELETED.
- Modify max clamp pressure = 3,000 kPa and reassess stiffness (30,000 Nm)

# Key EUV mask highlights (past 6 mo & Symp)



## **EUV Reticle Chucking Activities Ongoing**

- Un. Wisc continues modeling and empirical data matching to EUV blanks
- Precision tolerance mask ESC improvements are not meeting need.
- IOF precision chucks and Invax chuck improvements needed

## **P37, P38, and P40 modifications required and “Champions” needed**

- SEMI P37 is due for 5 year maintenance update, or it will expire in 2008. SEMI “micropatterning committee” needs lead chairs to update P37
  - P37 is obsolete as it is a “45nm” driven specification document
  - Changes needed to converge with P40 proposal from ASML
  - Known changes in local slopes, and non flatness terminology
- SEMI P38 update needed to support 5 year update in late 2008
  - Specs for absorber layers and thickness updated to converge with new data showing what aspect ratio for mask shadowing effects compensation
  -

# IEUVI Mask TWG Top Technical Issues 02/'07, 07/'07

	<i>Critical Issue</i>	<i>Status</i>	<u><i>Solution Path</i></u>
1	<b>Multilayer defect density (includes substrate)</b>		IBSD / Veeco development single path • 0.01 def/cm2 @ ≥ 40nm YE target
2	<b>Metrology / defect inspection; potential need for actinic inspection for blanks</b> • Optical inspection tool path to <30nm PSL • Actinic insp		3 <sup>rd</sup> generation inspection tool needed • What is the clear technology pathway (optical or actinic), business case • When / if consider actinic printing tool • Significant progress made on beta (30nm ML-4X)
3	<b>Patterned defect print</b>		...t needed ...ol dev. needed ...ffic ...t printing ...rm needed
4	<b>Handling &amp; masks</b>		...t needed ...ct sens. Tests Sema., Nikon ...n-Box C/N/E/A
5	<b>IP distortion included ML stress, and backside Cr layer requirements (adoption)</b>		...diversity of solutions approach by stakeholders.
6	<b>Patterned mask cleaning</b>		No new data; down in ranking due to other risks
6	<b>Substrate flatness and thickness variation</b>		Never been as clear that #5 & #6 are inter-related; first FS, BS, & LOTV data
8	<b>Multilayer repair for amplitude defects</b>		No new data; down in ranking due to other risks

**Critical Issues list reviewed and discussed extensively**

**Consensus that Critical Issue topics and rank order remains unchanged**

**Improved solution path for top 4 RED C.I.**

# IEUVI Mask TWG Top Technical Issues NOV '07 update

	<i>Critical Issue</i>	<i>Status</i>	<i><u>Solution Path</u></i>
1	<b>Multilayer defect density (includes substrate and phase defects)</b>		<i>IBSD / Veeco development single path</i> <ul style="list-style-type: none"> <li>• Need solution for substrate pits after ML is put on (pits are only visible after ML.</li> <li>• Do we need to do something to the pits before ML dep</li> </ul>
2	<b>Metrology / defect inspection; potential need for actinic inspection for blanks</b> <ul style="list-style-type: none"> <li>• Optical inspection tool path to &lt;30nm PSL</li> <li>• Actinic inspection tool path – commercialization</li> </ul>		<i>3<sup>rd</sup> generation inspection tool needed</i> <ul style="list-style-type: none"> <li>• <i>What is the clear technology pathway (optical or actinic), business case</i></li> <li>• <i>When / if consider actinic printing tool</i></li> <li>• <i>Significant progress made on beta</i></li> </ul> Excellent data from M7360 (40nm ML-4X) LBNL @λ , and MIRAI @λ <ul style="list-style-type: none"> <li>• 1<sup>st</sup> Qtr next year M7360 final sensitivity</li> <li>• Need 3<sup>rd</sup> generation inspection tool to cover 22nm HP requirements. Need to begin tool program now to have tool 2 years (need date). A.R. for consortia ?</li> </ul>
3	<b>Patterned mask defect inspection &amp; defect printability</b>		<i>12 month window assessment needed</i> <ul style="list-style-type: none"> <li>• <i>Pattern defect inspection tool dev. needed (evolution) – Non EUV specific</i></li> <li>• <i>Increased learning on experimental defect printing (resist, flare, shadowing included).</i></li> <li>• <i>Benchmark AIT with ADT (tool differences)</i></li> <li>• <i>Commercial EUV RIM platform needed</i></li> <li>• <i>DUV pattern inspection tools o.k. for now but will not be HVM 22nm capable.</i></li> </ul>



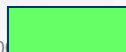
# IEUVI Mask TWG Top Technical Issues NOV '07 update

	<b>Critical Issue</b>	<b>Status</b>	<b><u>Solution Path</u></b>
<b>4</b>	<b>Handling &amp; protection of patterned masks</b>		<p>12 month window assessment needed</p> <ul style="list-style-type: none"> <li>• Pellicle concept (RR); Box-in-Box C/N/E/A</li> <li>• Very good improv. (&lt;1 def.) Sema., Nikon</li> <li>• 22nm HVM solutions require 25nm particle sens. tests</li> <li>• 50nm HP requirements are being worked but 32nm HP capability is issue</li> <li>• Initial partial data from F.F. tool(s) Feb '08</li> <li>• Backside particle inspection needed.</li> </ul>
<b>5</b>	<b>IP distortion caused by chucking, included ML stress, and backside Cr layer requirements (adoption)</b>		New incremental data being obtained through multiple organizations. Further work still needed
<b>6</b>	<b>Patterned mask cleaning</b>		New incremental data being obtained through multiple organizations. Further work still needed
<b>6</b>	<b>Substrate flatness and thickness variation</b>		#5 & #6 are inter-related; first FS, BS, & LOTV data. Material suppliers show some improvements but more work still needed
<b>8</b>	<b>Multilayer repair for amplitude defects</b>		No new data; down in ranking due to other risks

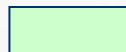
# IEUVI Mask TWG Improvement Roadmap (02/'07, 07/'07)

## EUV Substrates and Blanks

Parameter	Current Status	Alpha (2006 - 07)		Beta 32nm HP (2009 - 10)		Gamma '12-13 (32nm HP)	
		Spec.	Comments	Spec.	Comments	Spec.	Comments
Mean CTE (+ ppb/°K)	10	20	multiple suppliers (Corning, Ohara, etc.)	10	multiple suppliers (Corning, Ohara, etc.)	5	Corning & AGC claim SEMI P37-1102
CTE Spatial Var. (+ ppb/°K TIR)	10	10	multiple suppliers (Corning, Ohara, etc.)	8	Corning & AGC claim	6	SEMI P37-1102
Flatness Frontside (nm P-V)	<b>34nm (best)</b> 100nm (routine)	<b>100</b>	Commercial	<b>50</b>	34nm Commercial	<b>32</b>	SEMI P37-1102
Flatness Backside (nm P-V)	<b>39nm (best)</b> 100nm (routine)	<b>100</b>	Commercial	<b>50</b>	39nm Commercial	<b>32</b>	SEMI P37-1102
HSFR (nm rms)	<b>0.10 (best)</b> 0.13 (routine)	0.25	Commercial	0.2	Commercial	0.15	Commercial SEMI P37-1102
Front Surface Local Slope (mrad 3 $\sigma$ )	<b>0.8 (best)</b> 5.0 (routine)	5	Commercial	3	0.8 Commercial (Sematech / LBL report)	1.8	0.8 Commercial (Sematech / LBL report)
Substrate Total Defects @ PSL	<b>14 @ 53nm</b> LTEM (MBDC) 0 @ 43nm FS (MBDC)	50 @ 60nm	Commercial	10 @ 35nm	~0 @ 43nm PSL QZ (MBDC)	0 @ 30nm	SEMI P37-1102 (30nm PSL need)
Total ML D.D. (def./cm <sup>2</sup> @ PSL)	<b>0.025 @ 80nm</b> (MBDC) <b>0.09 @ 70nm</b> (MBDC) < 0.10 @ 80nm (Com.)	0.30	Veeco - SEMA. best [some Commer. cap.]	0.03	0.025 d/cm <sup>2</sup> @ 80nm Veeco at MBDC	0.003	SEMI P38-1103
Cut-off Size (PSL equivalent, nm)	<b>52nm</b> (ML) Lasertec M7360 <b>41nm</b> (sub) Lasertec M7360	80	Lasertec M1350	40	Lasertec M7360	25	SEMI P38-1103
Peak Refl. (%)	<b>65.0 (best)</b> 64.0 (routine)	<b>&gt;65.0</b>	Commercial	<b>&gt;66.0</b>	Veeco - SEMA. MBDC	<b>&gt;67.0</b>	SEMI P38-1103
Peak Refl. Unif. (%P-V) Absol.	<b>0.06 (best)</b> 0.40 (routine)	< 0.69	-Veeco - SEMA MBDC -Com. (SEMA report)	<b>&lt; 0.47</b>	-Veeco - SEMA MBDC -Com. (SEMA report)	<b>&lt; 0.33</b>	Commercial SEMI P38-1103
Median Central $\lambda$ Offset (nm)	<b>0.00 (best)</b> 0.04 (routine)	< +0.09	Commercial (SEMA report)	< $\pm$ 0.06	Commercial (SEMA report)	< $\pm$ 0.06	Commercial SEMI P38-1103
Reflected $\lambda$ Uniformity (nm P-V)	<b>0.022 (best)</b> 0.058 (routine)	0.08	Commercial (SEMA report)	<b>0.06</b>	Commercial (SEMA report)	<b>0.05</b>	Commercial SEMI P38-1103



Consistent capability



Demonstrated capability



Not demonstrated

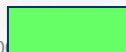


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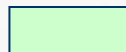
# IEUVI Mask TWG Improvement Roadmap Nov. '07 Update

## EUV Substrates and Blanks

Parameter	Current Status	Alpha (2006 - 07)		Beta 32nm HP (2009 - 10)		Gamma '12-13 (32nm HP)	
		Spec.	Comments	Spec.	Comments	Spec.	Comments
Mean CTE (± ppb/°K)	10	20	multiple suppliers (Corning, Ohara, etc.)	10	multiple suppliers (Corning, Ohara, etc.)	5	Corning & AGC claim SEMI P37-1102
CTE Spatial Var. (+ ppb/°K TIR)	10	10	multiple suppliers (Corning, Ohara, etc.)	8	Corning & AGC claim	6	SEMI P37-1102
Flatness Frontside (nm P-V)	<b>34nm (best)</b> 100nm (routine)	<b>100</b>	Commercial	<b>50</b>	34nm Commercial	<b>32</b>	SEMI P37-1102
Flatness Backside (nm P-V)	<b>39nm (best)</b> 100nm (routine)	<b>100</b>	Commercial	<b>50</b>	39nm Commercial	<b>32</b>	SEMI P37-1102
HSFR (nm rms)	<b>0.10 (best)</b> 0.13 (routine)	0.25	Commercial	0.2	Commercial	0.15	Commercial SEMI P37-1102
Front Surface Local Slope (mrad 3σ)	<b>0.8 (best)</b> 5.0 (routine)	5	Commercial	3	0.8 Commercial (Sematech / LBL report)	1.8	0.8 Commercial (Sematech / LBL report)
Substrate Total Defects @ PSL	<b>14 @ 53nm LTEM (MBDC)</b> <b>0 @ 30nm FS (MBDC)</b>	50 @ 60nm	Commercial	10 @ 35nm	<b>~0 @ 30nm PSL QZ (MBDC)</b>	0 @ 30nm	SEMI P37-1102 (30nm PSL need)
Total ML D.D. (def./cm <sup>2</sup> @ PSL)	<b>0.10 @ 56nm (MBDC)</b> ~ 0.2 @ 56nm (Com.)	0.30	Veeco - SEMA. best [some Commer. cap.]	0.03	<b>0.10 d/cm<sup>2</sup> @ 56nm Veeco at MBDC</b>	0.003	SEMI P38-1103
Cut-off Size (PSL equivalent, nm)	<b>50nm (ML) Lasertec M7360</b> <b>40nm (sub) Lasertec M7360</b>	80	Lasertec M1350	40	Lasertec M7360	25	SEMI P38-1103
Peak Refl. (%)	<b>65.0 (best)</b> 64.0 (routine)	<b>&gt;65.0</b>	Commercial	<b>&gt;66.0</b>	Veeco - SEMA. MBDC	<b>&gt;67.0</b>	SEMI P38-1103
Peak Refl. Unif. (%P-V) Absol.	<b>0.06 (best)</b> 0.40 (routine)	< 0.69	-Veeco - SEMA MBDC -Com. (SEMA report)	<b>&lt; 0.47</b>	-Veeco - SEMA MBDC -Com. (SEMA report)	<b>&lt; 0.33</b>	Commercial SEMI P38-1103
Median Central λ Offset (nm)	<b>0.00 (best)</b> 0.04 (routine)	< +0.09	Commercial (SEMA report)	< ±0.06	Commercial (SEMA report)	< ±0.06	Commercial SEMI P38-1103
Reflected λ Uniformity (nm P-V)	<b>0.022 (best)</b> 0.058 (routine)	0.08	Commercial (SEMA report)	<b>0.06</b>	Commercial (SEMA report)	<b>0.05</b>	Commercial SEMI P38-1103



Consistent capability



Demonstrated capability



Not demonstrated

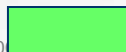


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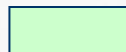
# IEUVI Mask TWG Improvement Roadmap (02/'07, 07/'07)

## EUV Masks and Mask Usage

Parameter	Current Status	Alpha		Beta (32nm HP beta tool)		Gamma (32nm HP)	
		Spec.	Comments	Spec.	Comments	Spec.	Comments
Nominal Image Size (4X)	150 nm	151nm	160nm NIS [AMTC] 150nm NIS [Intel]	120nm	160nm NIS [AMTC] 150nm NIS [Intel]	85nm	32nm HP (ITRS)
Min Primary Size DLS (4X)	60nm	106nm	89nm Min size [AMTC]; 100nm [Intel];100nm [DNP]	84nm	89nm Min size [AMTC]; 100nm [Intel]; 100nm [DNP]	59nm	32nm HP (ITRS)
Image Placement (nm 3s multipoint)	7.7 nm	8.0	7.7nm [AMTC]	4.5	5nm (x), 6nm (y); error EB only (NuFlare)	3.4	32nm HP (ITRS)
CD Mean To Target (nm)	3.5 nm	4.6	± 3.5nm [AMTC]	3.6	± 3.5nm [AMTC]	2.6	32nm HP (ITRS)
Linearity (nm)	5.0	8.7	5.0nm "iso to dense" linearity [AMTC]	6.8	5.0nm "iso to dense" linearity [AMTC]	4.9	32nm HP (ITRS)
CD Unif. IL MPU (3σ nm)	4.3 nm	5.0	7.9nm 3s (180nm) [AMTC] 4.3nm 3s (200nm) [DNP]	2.7		1.9	32nm HP (ITRS)
CD Unif. DLS (3σ nm)	4.1 nm	12.0	4.1nm 3s (180nm) [AMTC] 4.5nm 3s (200nm ) [DNP]	6.5	4.1nm 3s (180nm) [AMTC] 4.5nm 3s (200nm ) [DNP]	4.6	32nm HP (ITRS)
Absorber LER (3s nm)	2.0 nm	3.2	2.5nm (25 uC/cm <sup>2</sup> ) NuFla. 2.0nm (55 uC/cm <sup>2</sup> ) NuFla.	2.5	2.5nm (25 uC/cm <sup>2</sup> ) NuFla. 2.0nm (55 uC/cm <sup>2</sup> ) NuFla.	1.8	32nm HP (ITRS)
Reticle outgassing in vacuum H2O (mbar l/s after 10 hr)	1.78 X 10 <sup>-9</sup>	1.0 E-4	preliminary ASML performance	5.0 E-5		1.2 E-5	ASML proposal specs
Reticle outgassing in vacuum CxHy (mbar l/s after 10 hr)	2.35 x 10 <sup>-9</sup>	1.0 E-6	preliminary ASML performance	5.0 E-6		1.2 E-7	ASML proposal specs
Reticle outgassing in shipping H2O (mbar l/s after 10 hr)	1.78 X 10 <sup>-9</sup>	1.0 E-4	preliminary ASML performance	5.0 E-5		1.2 E-5	ASML proposal specs
Reticle outgassing in shipping CxHy (mbar l/s after 10 hr)	2.35 x 10 <sup>-9</sup>	1.0 E-6	preliminary ASML performance	5.0 E-6		1.2 E-7	ASML proposal specs
Added Particle per # handling events (@ PSL)	2 / 200 cycles 50nm	<1 / 100 @ 60nm	0 / 70 cycles 50nm [ASML]	<1 / 250 @ 45nm	2 / 200 @ 50nm (SELETE)	< ? per 500 @ 25nm	industry target spec needed
Added Particle per # shipping events (@ PSL)	0.5 @ 57nm	<2 / 100 @ 60nm	6 @ 50nm [SEMATECH - MBDC]	<2 / 100 @ 45nm	~0.50 @ 57nm (SEMA)	< ? per 500 @ 25nm	industry target spec needed



Consistent capability



Demonstrated capability



Not demonstrated



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# IEUVI Mask TWG Improvement Roadmap Nov. '07 Update

## EUV Masks and Mask Usage

Parameter	Current Status	Alpha		Beta (32nm HP beta tool)		Gamma (32nm HP)	
		Spec.	Comments	Spec.	Comments	Spec.	Comments
Nominal Image Size (4X)	150 nm	151nm	160nm NIS [AMTC] 150nm NIS [Intel]	120nm	160nm NIS [AMTC] 150nm NIS [Intel]	85nm	32nm HP (ITRS)
Min Primary Size DLS (4X)	60nm	106nm	89nm Min size [AMTC]; 100nm [Intel]; 100nm [DNP]	84nm	60nm [Intel]; 89nm Min size [AMTC]; 100nm [DNP]	59nm	32nm HP (ITRS)
Image Placement (nm 3s multipoint)	7.7 nm	8.0	7.7nm [AMTC]	4.5	5nm (x), 6nm (y); error EB only (NuFlare)	3.4	32nm HP (ITRS)
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Absorber LER (3s nm)	2.0 nm	3.2	2.5nm (25 uC/cm <sup>2</sup> ) NuFla. 2.0nm (55 uC/cm <sup>2</sup> ) NuFla.	2.5	2.5nm (25 uC/cm <sup>2</sup> ) NuFla. 2.0nm (55 uC/cm <sup>2</sup> ) NuFla.	1.8	32nm HP (ITRS)
Reticle outgassing in vacuum H2O (mbar l/s after 10 hr)	1.78 X 10-9	1.0 E-4	preliminary ASML performance	5.0 E-5		1.2 E-5	ASML proposal specs
Reticle outgassing in vacuum CxHy (mbar l/s after 10 hr)	2.35 x 10-9	1.0 E-6	preliminary ASML performance	5.0 E-6		1.2 E-7	ASML proposal specs
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Added Particle per # handling events (@ PSL)	0.5 / 100 cycles 50nm	<1 / 100 @ 60nm	0 / 70 cycles 50nm [ASML]	<1 / 250 @ 45nm	0.5 / 100 @ 50nm (SEMA)	< ? per 500 @ 25nm	industry target spec needed
Added Particle per # shipping events (@ PSL)	0.3 @ 50nm	<2 / 100 @ 60nm	6 @ 50nm [SEMATECH - MBDC]	<2 / 100 @ 45nm	0.30 @ 50nm (SEMA)	< ? per 500 @ 25nm	industry target spec needed

# Key Messages for the IEUVI Board (Nov 1. '07)

**Delta:** 3<sup>rd</sup> generation blank defect inspection tool program needs to begin now and must support 22nm HP. Funding and resources needed to begin program now (need date 2 years). Bottle neck for key solutions (cleaning, reticle handling, etc.)

**Delta:** Blank defect monitoring w/ DUV inspection is not enough; phase defects can print easily. Need phase defect inspection monitoring.

**Pro:** Blank defect reduction at MBDC and shown by supplier base is encouraging.

**Pro:** Cleaning performance demonstrated with 10nm particle removal and 0 particles of  $\geq 30$ nm

**Pro:** AIT improvements at LBNL with resolution down to 110nm at mask and illumination uniformity improvements.

**Pro:** Good increased learning on capping materials, pattern repair, and pattern printing impacts (Flare, shadowing, with initial empirical data, etc.)

**Delta:** Commercial RIM tool program needs to begin now and must be 22nm HP. Funding and resources needed to begin program now (need date 2 years).



# **2008 IEUVI MASK TWG**

**(in conjunction with SPIE Lithography)**

## **PROPOSED AGENDA ITEMS:**

### **– MASK PARTICLES / CONTAMINATION A SHOWSTOPPER?**

- Shipping, robotic handling, vacuum (Including echuck backside)

### **– MASK/eCHUCK FLATNESS**

- How are we doing versus SEMI spec
- Compensation by e-beam correction
- Backside particle impact
- What needs to change in the SEMI specs for both P37 and P40

# **2008 IEUVI MASK TWG (in conjunction with SPIE Lithography)**

## **PROPOSED AGENDA ITEMS:**

- Propose to have review meeting on carrier Yellow Ballot 4466 vote. Assess separate.**
- EUV Blank defect fiducial standards effort. Assess meeting timing.**

# IEUVI Mask TWG Report

## Back Up Materials



# What is the Objective of the IEUVI?

- **To coordinate collaboration among world EUVL consortia**
  - Align R&D activities to the International Technology Roadmap for Semiconductors (ITRS)
  - Coordinate R&D collaboration activities among consortia
- **To encourage coordination among suppliers**
- **Share progress reports**
- **Identify potential "show stoppers" for EUVL implementation**
- **Communicate implementation issues (e.g., to consortia, IC manufacturers, suppliers, and governments)**

# IEUVI Mask Technology Working Group (TWG)

## Mission Statements:

### **1. Provide a forum to support and foster improved EUV Mask Infrastructure Developments**

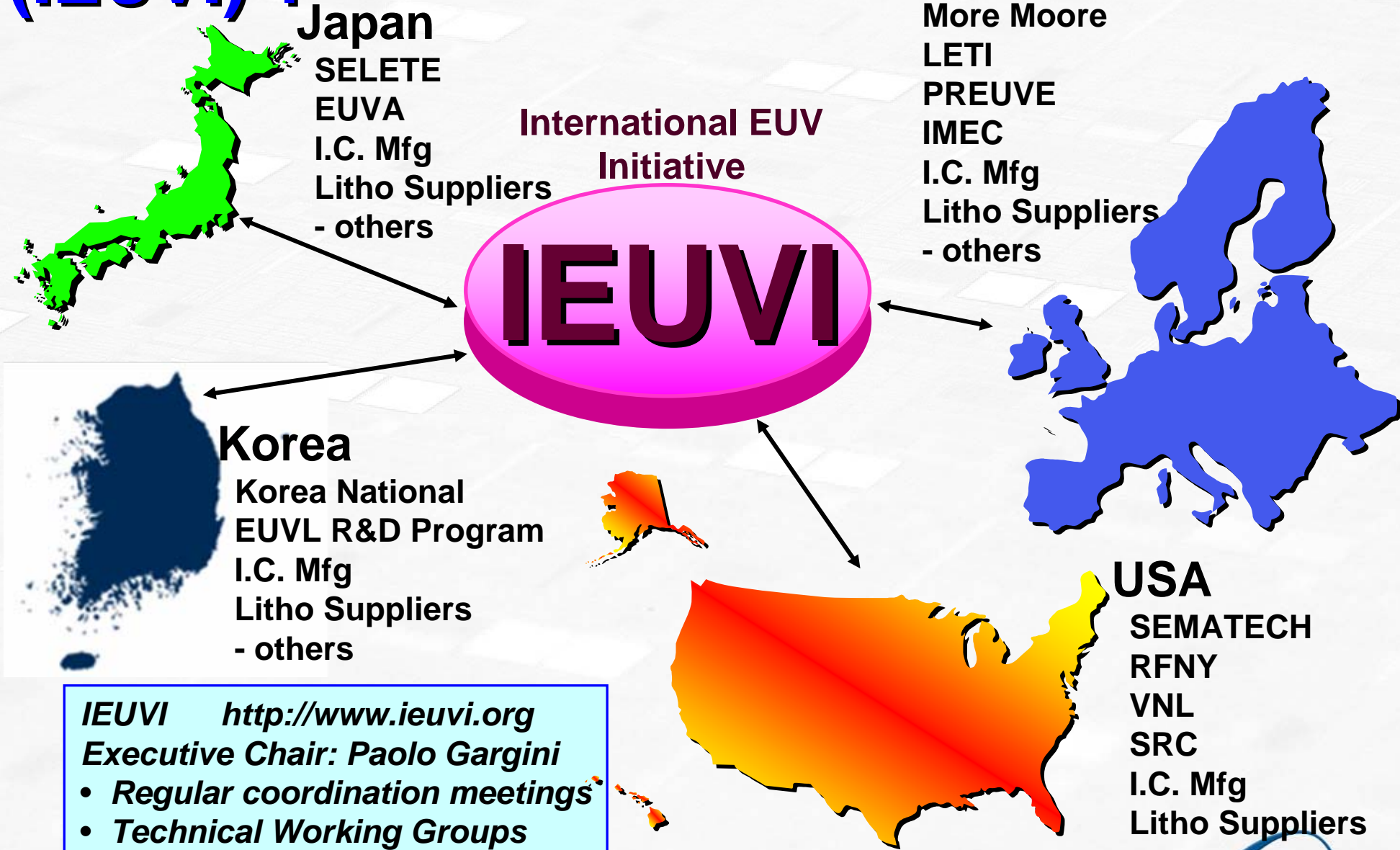
- Review key regional updates to IEUI Mask TWG representatives to improve global knowledge base (deter duplication of efforts where possible)
- Foster collaborative activity in key areas to reach consensus:
  - Commercial EUV Mask requirements
  - EUV mask standardization (e.g. carriers and handling)

### **2. Develop and agree to critical issues and needed progress versus requirements (roadmaps) to accelerate development**

- Assess continual progress and elevate key issues / showstopper items to correct industry levels
- Develop resolution plans or required activity to help provide solutions to key issues



# What is the International EUV Initiative (IEUVI) ?



**IEUVI** <http://www.ieuvi.org>  
**Executive Chair: Paolo Gargini**

- Regular coordination meetings
- Technical Working Groups
- Benchmarking data exchange
- Co-sponsorship of workshops



# What is the International EUV Initiative (IEUVI)?

IEUVI Source TWG

IEUVI Optics TWG



IEUVI Resist TWG

IEUVI Mask TWG

International EUV Initiative  
Executive Board  
(next meeting 11/02/07)

IEUVI  
<http://www.ieuvi.org>

**Executive Chair: Paolo Gargini**

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# Organizations working on EUV Masks

- ASML
- Corning Inc.
- Corning Tropel Corp.
- EUV Technology
- FALA Technologies
- FEI
- Invax
- KLA-Tencor
- Photronics
- QED Technology
- Rohwedder
- Toppan USA (DPI)
- Veeco
- Wave Optics
- Wave Precision
- EUV LLC
- RFNY
- SEMATECH
- SEMI
- SRC
- DARPA
- LBLN
- LLNL
- NIST
- SNL
- INVENT
- Northeastern Univ.
- U. at Albany, SUNY
- U. of Minnesota
- U. of Wisconsin



Many companies enter and exit EUV development community each year  
 Chart is hard to update 100% accurately.

- Asahi Glass
- AIST
- Canon
- Hakuto
- Hoya
- MIRAI
- Nikon
- Valqua
- HOYA
- DNP
- Toppan
- Hitachi High-Technologies
- JEOL
- NuFlare Technology
- Lasertec
- SOL
- Shin-Etsu chemical
- Tosoh
- Tosoh SGM
- Toshiba ceramics
- OHARA
- Kyocera
- Nitto Optical
- SELETE
- SEMI
- AIST
- Tohoku U.



- AIS
- Alcatel
- AMTC
- ASML
- Incam
- Leica
- Philips
- Roth & Rau
- Sagem
- Schott Glas
- SESO
- SOPRA
- ST Microelectronics
- imec
- More Moore
- CEA-LETI
- GREMI
- IOM
- IMS-CHIPS
- LORXN/L2MPI



## Korea

- Hanyang Univ.
- Seoul National Univ.
- POSTECH
- SKKU
- Pohang Accelerator Lab.
- Samsung Electronics
- Dongjin Semichem



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- Foster collaborative activity in key areas to reach consensus:
  - Commercial EUV Mask requirements
  - EUV mask standardization (e.g. carriers and handling)

### 2. Develop agreed to critical issues and needed progress versus requirements (roadmaps) to accelerate development

- Assess continual progress and elevate key issues / showstopper items to correct industry levels
- Develop resolution plans or required activity to help provide solutions to key issues



# IEUVI Mask TWG Activities

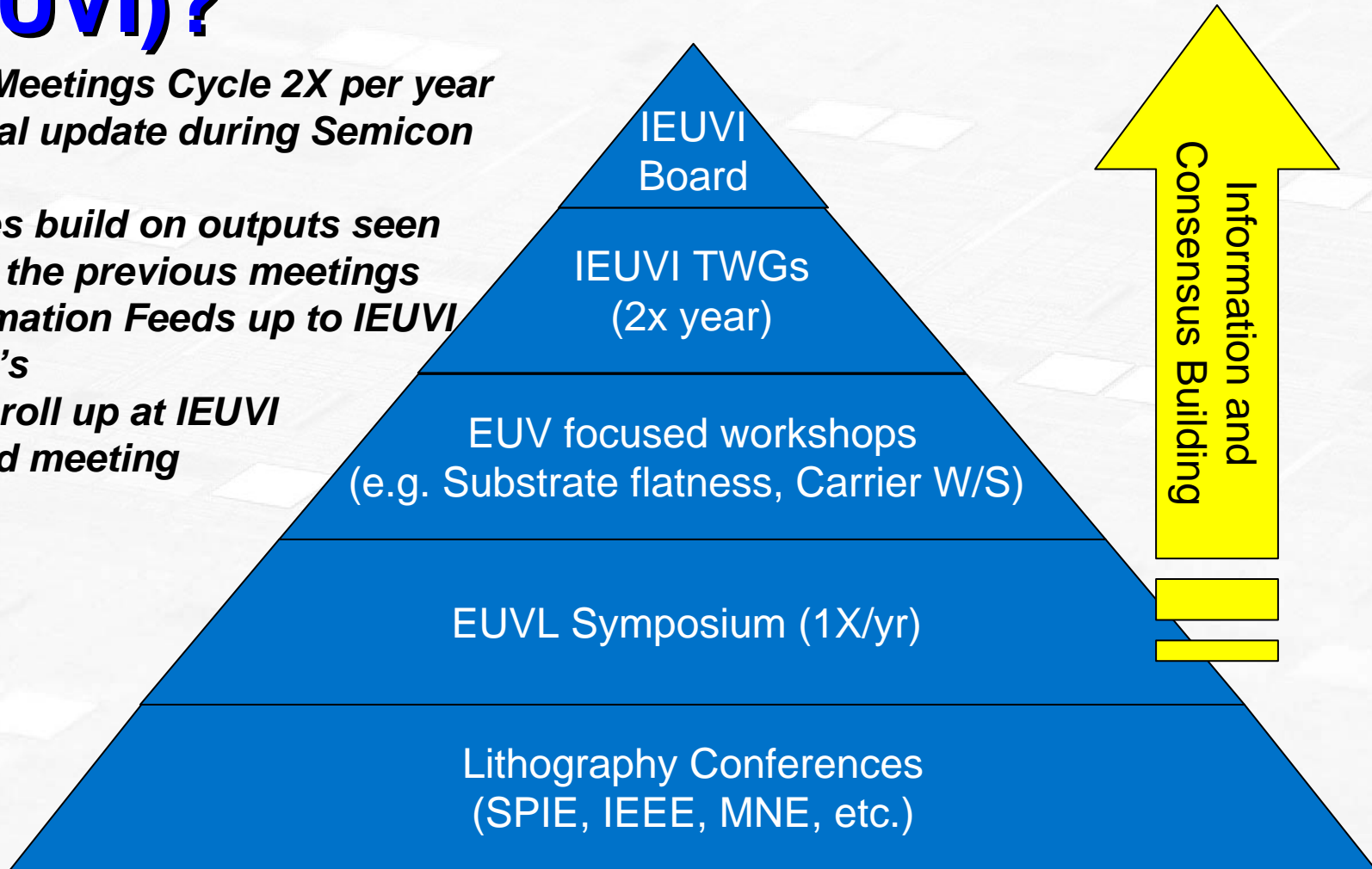
- **IEUVI Mask TWG top critical issues review (at least 2x year): current revision 11/2007**
  - Discuss in detail progress to date versus requirements
  - Re-rank list pending progress or additional issues uncovered
- **IEUVI Mask TWG roadmap specification updated regularly (at least 2x year): current revision 11/2007**
  - Assess “best achieved to date” (champion)
  - Assess capability at reasonable yields
- **Conduct surveys or coordinates inputs to other organizations (conducted on case – by – case need)**
  - Completed “gap funding” analysis for entire EUV mask infr. (Q2–Q4 ‘06)
  - Provided feedback and support of several standards activities
    - EUV Mask and Loadport SEMI Standard (SEMI 4466)
    - EUV blank fiducial for defect mitigation standardization (kick off Q1 ‘07)



# What is the International EUV Initiative (IEUVI)?

*IEUVI Meetings Cycle 2X per year*

- *Partial update during Semicon West*
- *Cycles build on outputs seen during the previous meetings*
- *Information Feeds up to IEUVI TWG's*
- *Final roll up at IEUVI Board meeting*



There are two full IEUVI meeting cycles per year

- Feb. / Mar. SPIE Advanced Litho (San Jose CA)
- EUVL Symposium Sep. / Oct. (International)
- ½ cycle partial update in July (IEUVI Board Telecon)