Intel perspective on EUV projection optics lifetime and contamination

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Lifetime specs

- Average stepper lifetime in a Fab is 8 – 10 years
  - Waterfalls from frontline to backend over lifetime
- Since 0.25 NA is going to be in development for 2, maybe even 3 process generations (32 nm node – 15 nm nodes)
  - So need to last from 2007 to 2011 or even 2013

Impact of contamination

- What does PO contamination in EUVL systems affect?
  - Degradation of peak reflectivity
    - 70% to 69% results in 85% of original source power (assuming 11 NI mirrors)
    - Affects throughput
  - Degradation of reflectivity uniformity
    - How much will this affect across field uniformity?
    - CD control budget for 32 nm node is 2.5 nm 3 sigma
  - Stress impact
    - Can result in across field figure errors, and hence impact CD uniformity
  - Affect flare? Not in same manner as DUV as EUVL is in vacuum
    - Impact of contamination TBD
  - Center wavelength shift
    - Impact of contamination TBD
- <u>Intel is more concerned about CD uniformity than a small decrease in throughput</u>

Solutions

- Prevention is better than cure
  - Reduce contaminants to zero
    - May not be guaranteed
    - Tighter specs on out-gassing proposed by Resist TWG
    - Out-gassing compounds include benzene etc [H. Cao et al, SPIE 2005]
  - Thermally stable MLs
    - Intel funded project with LLNL shows low stress and high peak reflectivity of ML with B4C inter-diffusion barrier
  - "Intelligent" capping layers
    - Intel believes that a ***large effort*** is needed to find a capping layer solution to the contamination problem
    - <u>Photo-catalytic materials</u> – materials which are stable to oxidation but get rid of hydrocarbons under EUV radiation
      - Intel funded projects in this area
- In-situ cleaning, only if necessary
  - Need to see credible data before implementation

Enabling activities that need to be addressed

- In-situ monitoring, preferably at all mirror surfaces is needed
- Accelerated lifetime testing at HVM fluxes is necessary
- Understanding degradation mechanisms of capping layers is required
- Learning from early tools
  - Integrated into future designs

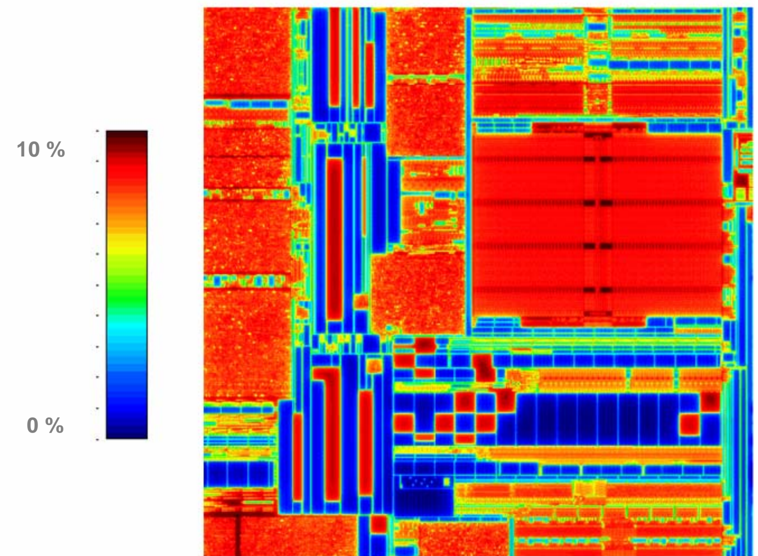
SEMATECH projects in this area need to be linked to supplier's programs

Back up slides

Systematic WID CD variation from sources such as flare could be compensated

- For a tool with 10% intrinsic flare, flare range on gate layer for typical microprocessor die is 6%*
- At 1.5 nm/%flare ** CD sensitivity, CD variation = 9 nm
- CD budget allocation to flare < 1 nm

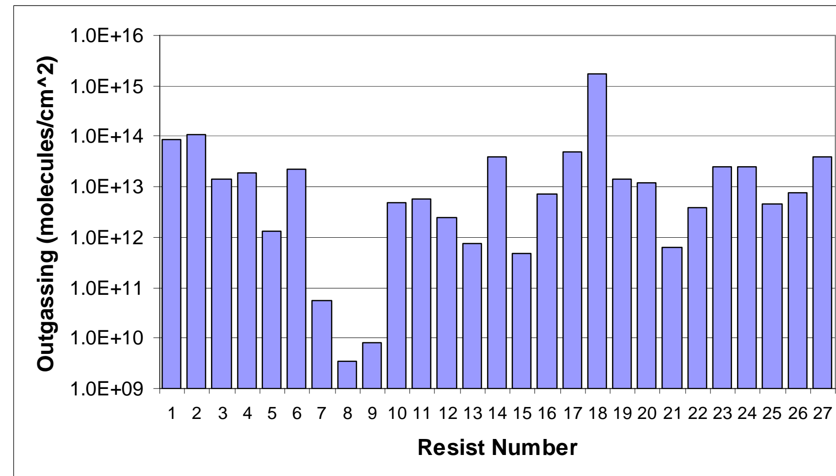
$\therefore$ Flare Variation Compensation (FVC) is required



Convolution of a scaled PSFsc for POB2 with Intel microprocessor gate layer

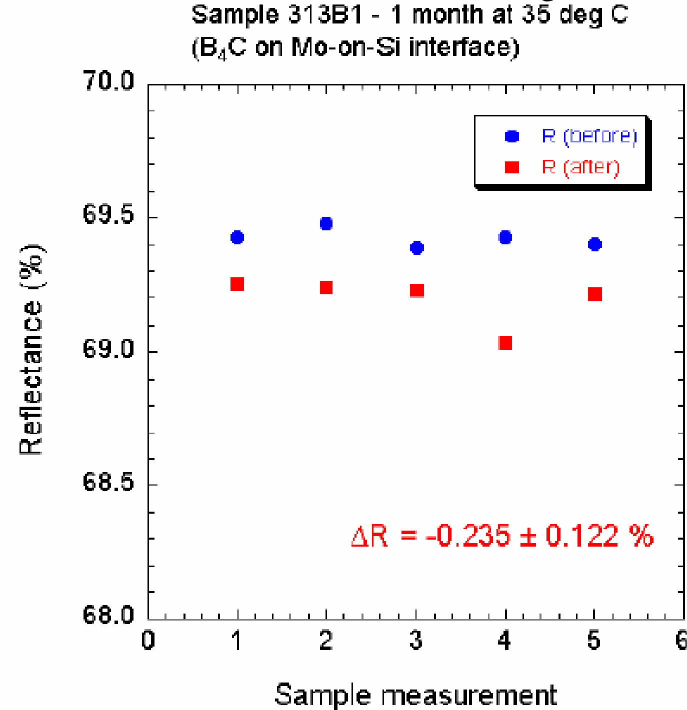
*Excluding areas that are completely dark or clear
** Measured on the ETS using EUV-2D

Resist outgassing specs



- Outgassing limit for Intel MET 6 $*10^{13}$ molecules/cm^2
- Proposed outgassing limit for EUV HVM tools $1 * 10^{10} - 1 * 10^{11}$ molecules/cm^2

Reflectivity of thermally stable MLs



- Peak reflectivity > 69% with B_4C diffusion barrier and Ru capping layer achieved on Si substrates
- Finish quality on mirror substrates needs to be ~ 0.15 nm to achieve same results
  - Difficult to achieve without compromising on figure and MSFR.